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Efficiency analysis of a modular H-bridge based on *SiC* MOSFET

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ABSTRACT

Several new high-performance power semiconductors have appeared during the last decade, being the silicon carbide (*SiC*) MOSFETs the most promising to be commercialised as an alternative of Si IGBT. This paper presents the performance analysis of a controller for a full H-bridge based on *SiC* MOSFET technology used for high frequency and medium voltage applications. The switching performance of a modular H-bridge is analysed and the efficiency/losses and temperature dissipation are experimentally measured in order to help engineers to design and develop circuits using this power semiconductor. A comparison between *SiC* MOSFET and Si MOSFET is also presented.

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Modular H-bridge; *SiC*-MOSFET; efficiency analysis

1. Introduction

Silicon carbide (*SiC*) MOSFETs have been attracted as a superior alternative for power switching devices because they offers several advantageous electrical characteristics such as lower on-resistance, higher temperature durability, higher speed switching performance and lower switching losses compared to Si IGBT (Mukunoki et al., 2016). These features allow the use of *SiC* MOSFETs for the development of more efficient systems that have been applied in recent years in many applications such as matrix converters (Safari, Castellazzi, & Wheeler, 2014), multilevel converters (Wu, Qin, Saeedifard, Wasynczuk, & Shenai, 2015), inverters (Gurpinar & Castellazzi, 2016) and DC/DC converters (Nakakohara et al., 2016). To exploit the features of the *SiC* MOSFET devices, the designers must know the technical limitations of the *SiC* MOSFET because the efficiency of the power devices have a very significant impact on the performance of the final system implemented. For example, a high switching frequency produces lower total harmonic distortion values, however the negative effect is that the switching power losses increase significantly at high frequencies. The ability to operate at high switching frequencies with reduced switching power losses is one of the features that differentiate *SiC* MOSFET from other mass-use switching devices.

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Although published results show the interest of the use of *SiC* MOSFET devices in several applications, they do not present a detailed performance analysis of the device (Tanabe et al., 2015, June; Yin, Tseng, Simanjorang, & Tu, 2017). Few comparative study between *SiC*-MOSFET and IGBT can be found in (Trentin, de Lillo, Empringham, Wheeler, & Clare 2015; Trentin et al., 2016) applying to matrix converters. In this context, the main contribution of this paper is the experimental efficiency/losses and thermographic analysis of the power device *SiC* MOSFET, using a modular H-bridge as a case study. Furthermore, a comparison between *SiC* MOSFET and *Si* MOSFET is also presented.

2. Description of the full H-bridge topology and experimental system

The block diagram of the H-bridge is shown in Figure 1(a). The control signals for the H-Bridge scheme are sent by two fibre-optic links whose signals are processed by the HFBR-2521Z fibre optic receiver (Figure 1(b). Then, the two electrical PWM signals are sent to a block in charge of generating the complementary $\overline{\text{PWM}}$ signals necessary for the control of each branch of the H-bridge. This circuit also implements the necessary dead time between each PWM and its complement $\overline{\text{PWM}}$, which is performed by using XOR 74HC86 gates and resistive and capacitive elements. The driver for *SiC* MOSFETs is implemented using the IR2110S integrated circuit, as shown in Figure 1(c). For the assembly of the power stage of the design, the *SiC* MOSFET SCH2080KE, shown in Figure 1(d) is used. In order to achieve the modularity of each H-bridge cell, they have their own independent power source (VCC_1 and VCC_2) implemented by the galvanically isolated DC/DC converter CC10-1212SF (Figure 1(e)).

Figure 2(a) shows the experimental platform used for the tests. An *RL* load with values of $R = 20\ \Omega$ and $L = 10\ \mu$H was used for the analysis.

Voltage measurements were performed with a Tektronix P5210A voltage differential probe, while the currents were measured using a Tektronix TCPA300 current probe. A

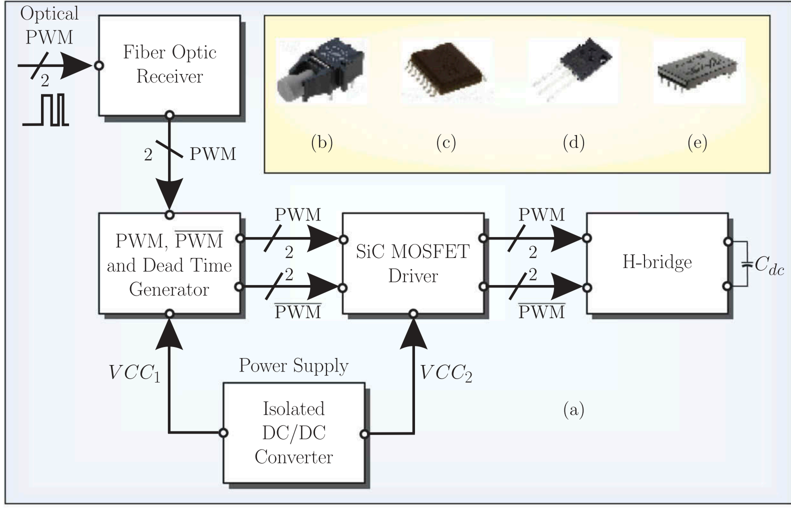

Figure 1. Block diagram of the H-bridge driver and its components.

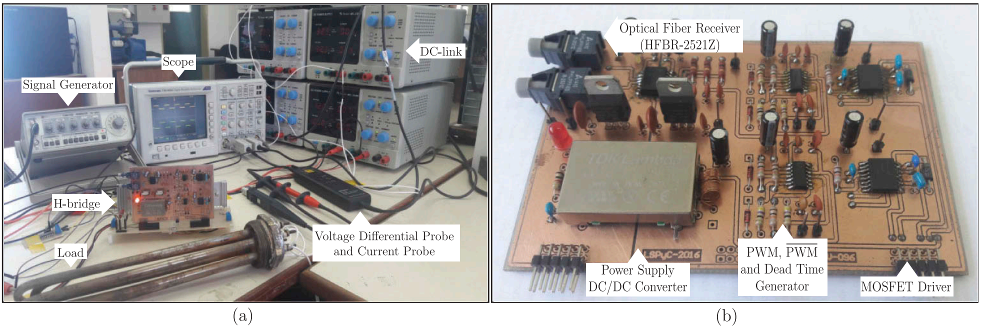

Figure 2. Experimental system: (a) measurement test rig setup, (b) H-bridge driver.

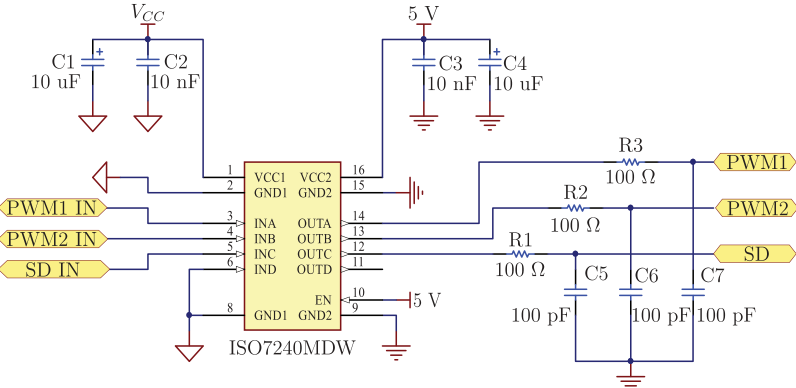

Figure 3. Conditioning circuit for PWM input signal with galvanic isolation and passive *RC* output filters.

variable DC-link was implemented by using several DC power sources Minipa model MPL-3305M, to capture the signals used a Tektronix digital oscilloscope model TDS3034C. The test signal was obtained from an EX Digital generator model FG-8002. Figure 2(b) shows the final design of the modular H-bridge.

Once the signal obtained by the fibre optic link has been processed, it is necessary to perform the conditioning of the PWM signal used to control the *SiC*-MOSFET shots, which signals are overlapping during high- or low-level transitions. The signal matching is implemented using the ISO7240 integrated circuit; these digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide insulation barrier (SiO_2). Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local reference and damaging or interfering with sensitive circuits. These devices have input thresholds with TTL levels and require two power voltages (3.3 V or 5 V). Figure 3 shows the circuit diagram designed to perform the conditioning of received PWM signals by using Altium Designer software.

3. Experimental results

Several experimental analyses were performed in order to analyse the modular H-bridge based on *SiC* MOSFET as well as a comparison with the same H-bridge but using a Si MOSFET. The diagram of the experimental platform implemented for the measurements is shown in Figure 4. The PWM signals are sent through the fibre optic link to the H-bridge controller, voltage and current measurements are made in the *RL* load, as well as measurements of the switching devices.

Figure 5 shows the PWM and $\overline{\text{PWM}}$ signals, where the dead time value is 1 μs for a frequency 100 kHz. This dead time is obtained by a circuit composed of logic gates 74HC86 and resistive and capacitive elements. The output voltage (V_o) and output current (I_o) are shown in Figure 6. Note that I_o has a slower transitions between high and low levels compared with V_o due to the inductive nature of the load.

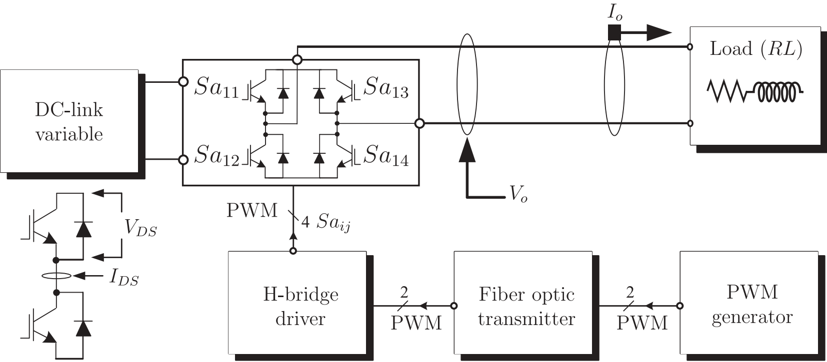

Figure 4. Diagram of the experimental platform implemented for the realisation of the measurements.

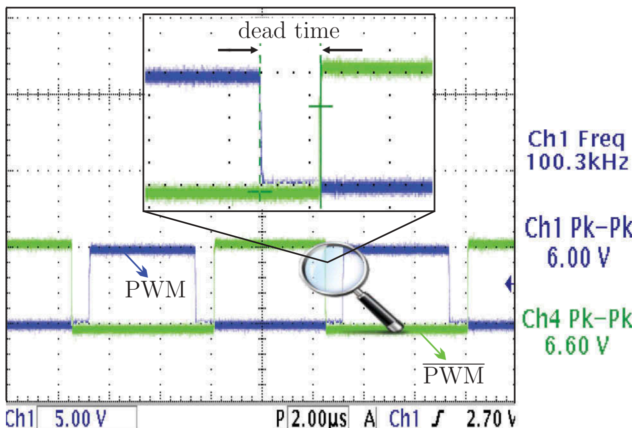

Figure 5. PWM and $\overline{\text{PWM}}$ signals and dead time (Ch1: PWM voltage–5 V/div; Ch2: $\overline{\text{PWM}}$ voltage – 5 V/div).

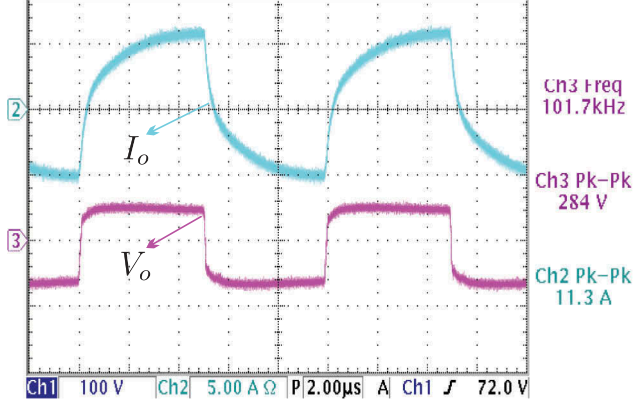

Figure 6. Output voltage (V_o) and output current (I_o) delivered to the *RL* load at 1 kW (Ch1: output voltage–100 V/div; Ch2: output current – 5 A/div).

In order to calculate the efficiency of the proposed modular full H-bridge the following equations are used for the conduction losses (Equation (1)) and switching losses (Equation (2)) presented by the *SiC* MOSFET (Wang et al., 2016):

$$P_{CM} = V_{DS}\, I_{Drms} = R_{DS(on)}\, I^2_{Drms} \tag{1}$$

$$P_{sw} = \frac{V_{DD}\, I_D}{2}(t_{on} + t_{off}) f_s \tag{2}$$

being f_s the operating frequency, I_{Drms} the drain current root-mean squared (rms), $R_{DS(on)}$ the drain source resistance, V_{DD} the DC-link voltage, t_{on} and t_{off} the state transition time intervals, turn-on and turn-off, respectively. It is, therefore, necessary to measure the variables in equations (1) and (2) (see Figure 7).

Then, some tests have been carried out varying the output power (0.5 kW and 1 kW) as well as the switching frequency (from 50 kHz to 200 kHz). According to the obtained results (Figure 8), the global losses increase with frequency while the efficiency

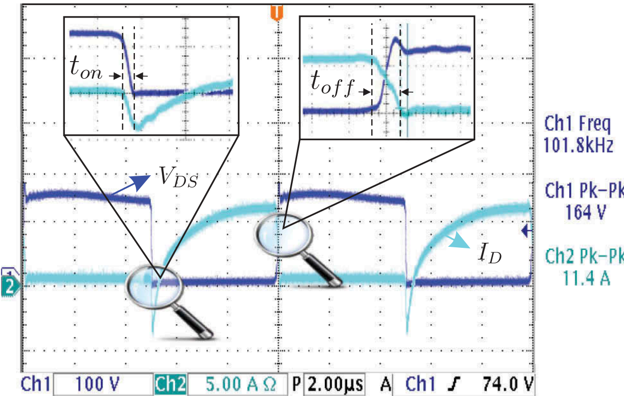

Figure 7. Modular H-bridge switching characteristics at 1 kW (Ch1: drain-source voltage – 100 V/div; Ch2: drain current – 5 A/div).

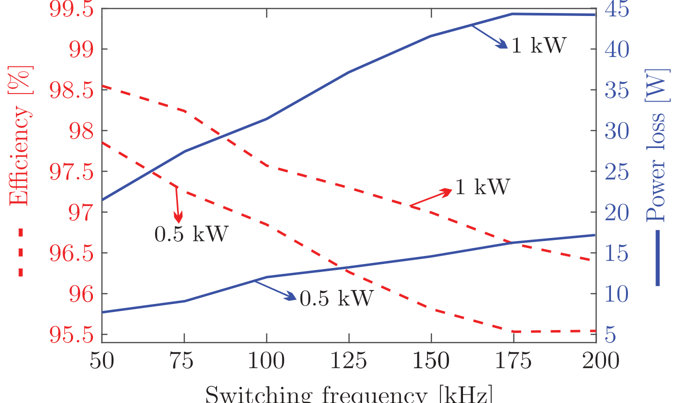

Figure 8. Efficiency (cut lines) and power losses (continuous lines) regarding the switching frequency.

decreases with the increase of the switching frequency. Notice that the efficiency is more than 95.5% for all analysed cases, being at 50 kHz the highest 98.5% efficiency for 1 kW of output power.

Then, it is interesting to make a thermal quantification of the *SiC* MOSFETs. Figure 9 shows a photograph obtained by a thermal imaging camera, being the temperatures on the *SiC* MOSFETs $SP_1 = 75.3°C$, $SP_2 = 72.1°C$, $SP_3 = 76.3°C$, $SP_4 = 69.4°C$. By a thermographic analysis it is possible to predict failure or malfunction points by non-uniform temperature as well as noting points of overheating. In this case the heating of each *SiC* MOSFET is approximately 7°C difference between the lower heating point with respect to greater heating. These measurements are important in determining the points of greatest stress with respect to the power dissipation in the modular H-bridge design.

To conclude the efficiency analysis, a comparative study between the *SiC* MOSFET and the Si MOFSFET is performed. Some important specifications of both state-of-the-art power semiconductors are listed in Table 1. For this test, a DC current flowing in the

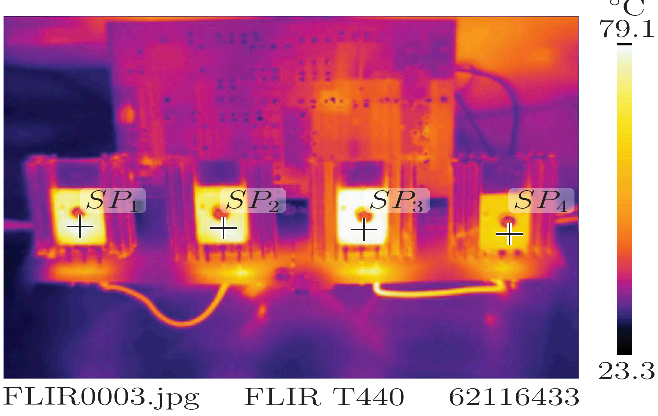

Figure 9. Thermographic image obtained from the H-bridge implemented with *SiC* MOSFETs.

Table 1. Specifications of *SiC* MOSFET and Si MOSFET.

Parameter	Unit	*SiC*-MOSFET	Si-MOSFET
Drain-to-source breakdown voltage	[V]	1 200	40
Static drain-to-source on-resistance	[mΩ]	80	1.4
Continuous drain current	[A]	40	195
Maximum power dissipation	[W]	262	375
Turn-on delay time	[ns]	37	65
Rise time	[ns]	33	827
Turn-off delay time	[ns]	70	97
Fall time	[ns]	28	355
Input capacitance	[pF]	1 850	10 315

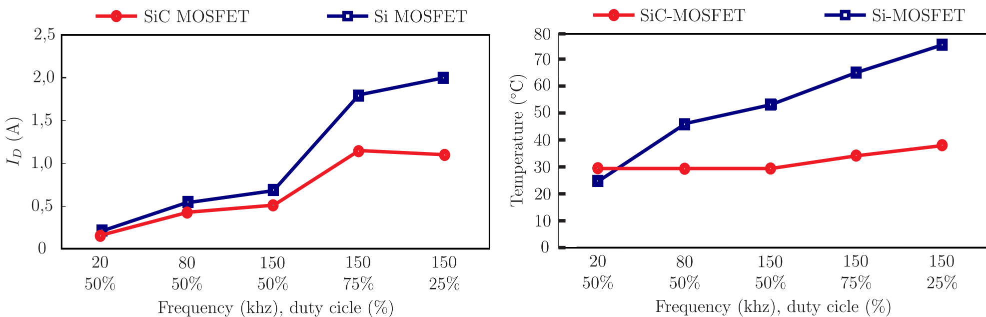

Figure 10. Comparison between *SiC* MOSFET and Si MOSFET. (a) Drain current and (b) temperature analysis.

H-bridge driver is plotted in Figure 10(a) against PWM frequency and duty cycle. The red and blue lines indicate currents of *SiC* MOSFET and Si MOSFET H-bridge drivers, respectively. The load was the solar linear motor connected to each H-bridge driver by the same condition. Then the cause of the current difference is attributed to the device, where the SIMOSFET has less R_{DSon} than the *SIC* MOSFET. As shown in Table 1, the response time of the *SiC* MOSFET is considerably lower than that of the SI MOSFET, whereby the *SIC* MOSFET develops lower power dissipation due to the switching losses. The currents at 150 kHz and with a duty cycle of 25 % is 1.1 A and 2.0 A for *SiC* MOSFET and Si MOSFET, respectively. Temperature rise of each device is plotted in Figure 10(b) similar to Figure 10(a). The temperature at 150 kHz and with a duty cycle of 25 % was 39°C and 76°C for *SiC* MOSFET and Si MOSFET, respectively. There is a big difference in temperature rise at high frequencies.

4. Conclusion

In this paper, the design and efficiency analysis of a modular H-bridge based on *SiC* MOSFET is presented. Experimental results show that the switching losses increase with frequency while conduction losses decrease with frequency. Switching losses in its transition from low to high represent the 92% of losses, while the transition from high to low represents the 2%. The conduction losses accounted for 6% of total losses. The design responds appropriately within the range of operating frequencies

ranging between 50 and 200 kHz, yielding an efficiency from 98% to 95% with increasing frequency. According to the experimental results for the comparison between *SiC* MOSFET with Si MOSFET by using normal H-bride driver, temperature rise at high PWM frequencies was the most prominent difference between them. Considering that the PWM frequencies tested were 20 kHz up to 156 kHz and duty cycles were 25%, 50% and 75%, the highest temperatures were 39°C and 76°C for *SiC* MOSFET and Si MOSFET, respectively, both at PWM frequency of 150 kHz and duty cycle of 25%.

Disclosure statement

No potential conflict of interest was reported by the authors.

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