

Article

A SiC-MOSFET Bidirectional Switch Solution for Direct Matrix Converter Topologies

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Abstract

Bidirectional switches are highly required power electronics units for the design of power converters, especially for direct matrix converters. This article presents the design and implementation of a compact bidirectional switch based on SiC-MOSFET technology, aimed at high-efficiency, high-density power electronics applications. The proposed architecture employs surface-mount components, optimizing both the occupied area and electrical performance. The selected switching device is the IMBG120R053M2H from Infineon, a SiC-MOSFET known for its low on-resistance, high reverse-voltage blocking capability, and excellent switching speed. To drive the power devices, the UCC21521 gate driver integrates two independent isolated outputs in a single package, enabling precise control and reduced electromagnetic interference (EMI). The developed design supports bidirectional current conduction and voltage blocking, offering a robust and scalable solution for next-generation power converters. Design criteria, simulation results, and experimental validations are discussed.

Keywords: bidirectional switch; power converter; SiC-MOSFET; MOSFET drive



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1. Introduction

In recent decades, the growing demand for electrical energy has practically necessitated advances in the technologies used in electrical energy conversion systems across various areas. This aims to enhance their effectiveness and efficiency in technical operations, as well as improve system energy efficiency. These conversion systems are primarily based on Power Electronic Converters (PECs), which are widely used in various areas, including electric transportation, electric machine drives, distributed renewable generation, and microgrids, among others [1–4]. These PECs come in the form of inverter converters such as Voltage Source Inverters (VSIs), DC-DC converters, as well as AC-AC converters such as Back-to-Back (BtB) or Matrix Converters (MCs), the latter of which has been widely

developed in recent years due to its advantage in not including energy storage elements for the conversion [5,6].

MCs inherently employ semiconductor switches of various types, such as those from the MOSFET family (e.g., silicon (Si-MOSFET) for applications that do not require high power) and those from the IGBT family (for slightly higher-power applications). The challenge of seeking maximum effectiveness and efficiency in PECs has driven researchers to develop semiconductor devices based on new technologies [7]. These include MOSFET switches based on silicon carbide semiconductors (SiC-MOSFET). These have advantages over traditionally used devices, such as Si-MOSFETs, and include IGBTs, such as Si-IGBTs or RB-IGBTs [8–10]. Among the benefits of SiC-MOSFETs are the ability to operate at a higher switching frequency and greater power than Si-MOSFETs, as well as having lower switching losses, better temperature dissipation and greater switching capacity at high frequencies compared to the traditionally used IGBTs or MOSFETs [11].

Regarding the types or configurations of switching devices, bidirectional switches (Bi-Sw) are well-known and widely used in MCs and PECs. These devices, also known as four-quadrant switches, allow current to flow in both directions and handle both positive and negative voltages [12]. This bidirectionality offers an advantage over their implementation in MCs, enabling applications such as regenerative braking in electric vehicles and microgrids in distributed generation with grid interconnection. At the same time, this ensures losses are kept to the lowest possible magnitude [13,14]. In this context, this article focuses on proposing a high-power optimized Bi-Sw design for use in MCs, which combines design compactness with the high energy efficiency and high frequency switching capability typical of SiC-MOSFET semiconductor switches, as an attractive alternative to the constant search for minimizing energy losses in MCs and miniaturizing their component elements. All these features remain valid regardless of the control technique that may be used, making the design versatile and universal in terms of control strategies. Taking this into account, the main contribution of this article is the design of a compact, effective, and efficient SiC-MOSFET-based bidirectional switch for MC applications, providing the required design details. This article is organized as follows: Section 2 presents an overview of a bidirectional switch based on SiC-MOSFET transistors. Section 3 describes the bidirectional switch design for each stage. Section 4 presents the calculations and analysis criteria to be considered for the design. Section 5 presents the experimental implementation framework and the main results; and finally, Section 6 presents the conclusions.

2. Bidirectional Switch Overview

Bidirectional switches (Bi-Sw) are electronic devices capable of controlling current flow in both directions; in other words, they can conduct current bidirectionally, hence the name [15]. Figure 1 shows the topology of a Bi-Sw, consisting of two power transistors connected in an antiparallel configuration. Each power transistor can conduct current in only one direction. For this reason, Bi-Sw devices are highly specific and are not commonly available on the commercial market. That is why it is necessary to design a custom Bi-Sw to implement the power converters.

The design and implementation of the Bi-Sw is based on SiC-MOSFETs. This development aims to enhance the efficiency and switching capability of power devices, enabling superior performance in high-frequency and high-voltage applications [7,8]. Advances in SiC technology have led to greater energy efficiency, significant reductions in switching losses, and improved device reliability, making them ideal for applications in power conversion, transmission systems, and power electronics in general [15].

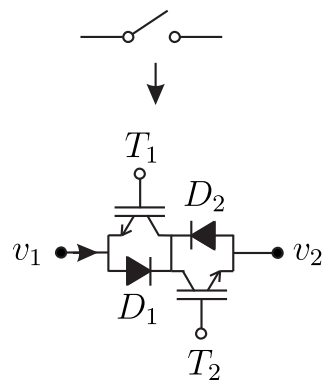


Figure 1. Bidirectional switch topology.

The Bi-Sw design is divided into two modules: the driver stage and the power stage. The driver stage performs signal conditioning to match the voltage and current levels required by the power device, thus ensuring correct operation and electrical noise isolation. The power stage consists of a SiC-MOSFET, which switches the AC input voltage. The power stage consists of the SiC-MOSFET, which switches the AC input voltage. Figure 2 shows the block diagram of the Bi-Sw, which includes a PWM generator, as well as the driver and power stages, respectively. Switching devices require a gate signal to define their ON and OFF states. In most applications, this signal is generated by a PWM signal, developed by control algorithms implemented on microcontrollers, DSP, or FPGA.

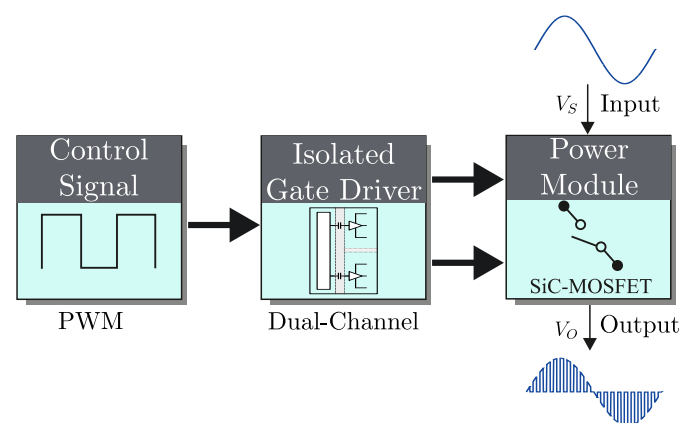


Figure 2. Block diagram of the operating principle of the bi-directional switch (Bi-Sw).

The main objective of this design is to develop a compact and efficient Bi-Sw that can be integrated into high-performance MCs.

3. Description of the Bidirectional Switch Design

The design of the proposed Bi-Sw is presented in Figure 3, which was developed using KiCad Version 9.0.0 software. The control stage, Figure 3a, processes the gate signals received from the external control system and provides the appropriate pulses to drive the power devices. To achieve this, galvanic isolation is ensured between the control logic and the power stage, reducing the risk of electrical transients and improving noise immunity. This stage is essential for providing reliable, bidirectional switching.

The power stage, seen in Figure 3b, consists of switching devices based on silicon carbide (SiC) technology, selected for their favorable characteristics in terms of efficiency, blocking capacity, and switching speed. This stage is directly responsible for power management and has been designed to minimize losses, improve dynamic response, and withstand demanding operating conditions. Finally, the printed circuit board (PCB) layout was de-

signed to efficiently integrate both functional blocks, ensuring good thermal and electrical performance. Design techniques were applied to reduce parasitic inductance, optimize current distribution, and facilitate assembly with SMD components. The entire system was developed using KiCad, which enabled the design of both the electrical schematic and PCB layout with a high degree of control over critical routing.

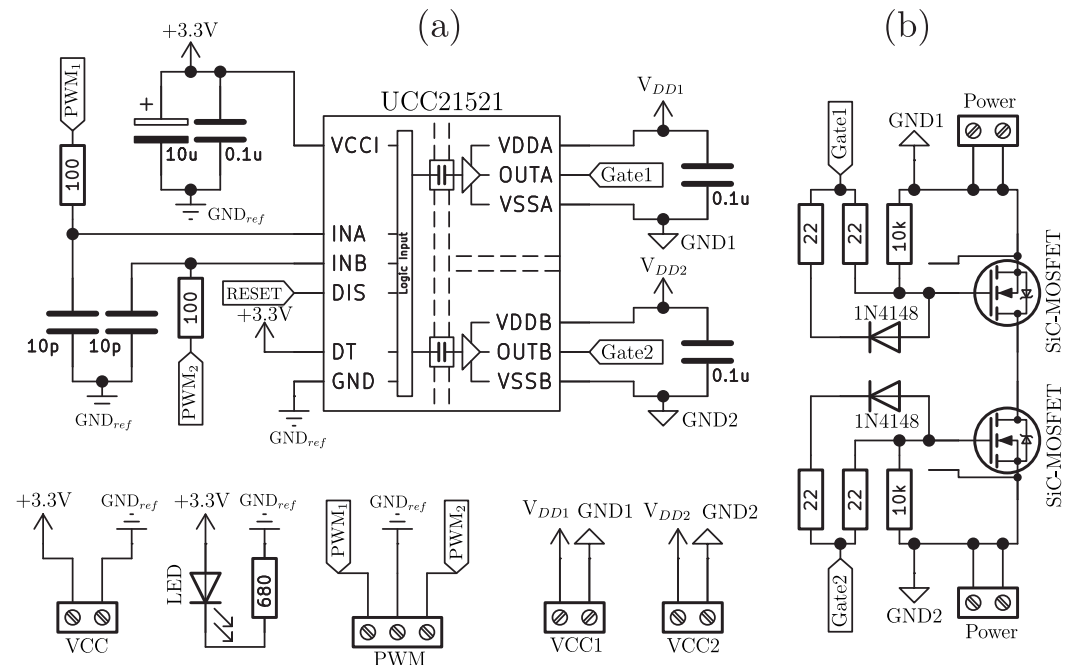


Figure 3. Electrical schematic of the Bi-Sw using KiCad EDA software, (a) driver stage and (b) power stage.

3.1. Driver Stage Design with Galvanic Isolation

The main function of the driver stage is to generate the gate signals required to properly activate the power transistors while ensuring electrical isolation between the control system and the power stage. This galvanic isolation is essential to protect the system from disturbances originating on the power side, such as high-voltage transients, current spikes, or electromagnetic noise, which could compromise the integrity of the control circuit. To meet these requirements, the UCC21521 gate driver of the Texas Instruments was selected [16]. This is a dual-channel driver with integrated isolation, allowing independent operation of two switching devices. It features reinforced isolation based on capacitive technology, with a withstand voltage of up to 5.7 kVrms, suitable for high-energy switching applications. Its high common-mode transient immunity (CMTI > 100 V/ns) makes it a robust solution for environments with fast switching and high voltage gradients. According to the specifications in Table 1, the UCC21521 can operate with an input supply voltage (V_{CCI}) ranging from 3 to 5.5 V, ideal for control logic systems based on microcontrollers or DSPs. On the output side (V_{DD1} and V_{DD2}), which drive the power devices' gates, the operating range is 13 to 20 V, providing flexibility in the design of the gate-drive circuit. Additionally, the driver offers an output current capability of 4 to 6 A, sufficient to handle the gate capacitive loads associated with SiC-MOSFETs, even during fast transitions. Another notable technical feature is its ability to operate at frequencies above 2 MHz, making it suitable for high-speed switching applications. This is complemented by low propagation delay and minimal pulse distortion—critical factors when precise synchronization is required between complementary signals or between parallel branches in multipath configurations. Figure 3a shows the electrical schematic of the control stage, highlighting the symmetrical configuration around the UCC21521, with separate inputs for each channel (INA and INB) and independent outputs for driving

each MOSFET. The suffixes 1 and 2 are used to differentiate the power transistor's feeds and signals, respectively. Gate resistors, clamping diodes, and decoupling capacitors can also be seen at the driver outputs; these elements serve to limit overvoltages, dampen oscillations, and preserve signal integrity under transient conditions. The adopted topology enables practical bidirectional switching, ensuring that each transistor can be individually controlled without mutual interference. Furthermore, the design was carried out with careful consideration of ground loop minimization and reduction of parasitic coupling between channels to ensure stable operation.

Table 1. Technical specifications of the UCC21521.

Parameter	Symbol	Value	Unit
Input supply voltage (control side)	V_{CCI}	3–5.5	V
Output supply voltage (power side)	V_{DD1}, V_{DD2}	13–20	V
Isolation voltage	—	5.7	kV _{rms}
Output current capability	—	4–6	A
Operating temperature range	—	−40 to 125	°C
Maximum switching frequency	—	>2	MHz

3.2. Power Stage Design with SiC-MOSFET

The power stage of the Bi-Sw is responsible for efficient switching of the electrical current, allowing both current conduction and voltage blocking in both directions. For this purpose, second-generation SiC-MOSFETs were selected, specifically the IMBG120R053M2H model from Infineon [17], part of the CoolSiC™ family, which offers advanced characteristics in terms of blocking capability, low on-state resistance, and thermal robustness. Its inclusion enables high efficiency levels and operation at elevated switching frequencies, while maintaining controlled thermal dissipation even under demanding conditions. As shown in Table 2, this device supports a drain-source voltage (V_{DS}) of up to 1200 V, providing a wide operating margin against possible overvoltages in grid-connected systems. Its on-state drain-source resistance ($R_{DS(on)}$) is only 52.6 mΩ at 25 °C, minimizing conduction losses during operation. Additionally, it features a gate threshold voltage ($V_{GS(th)}$) of 4.2 V, and a recommended turn-on voltage ($V_{GS(on)}$) in the range of 15 V to 18 V, which is compatible with the levels supplied by the control stage. The MOSFET also features a short-circuit withstand time (t_{SC}) of 2 μs which, although limited, provides a degree of protection under fault conditions. Its maximum junction temperature under overload (T_{vj}) reaches 200 °C, reflecting its ability to operate in high-thermal-density environments—particularly important in compact designs where heat flow must be managed efficiently.

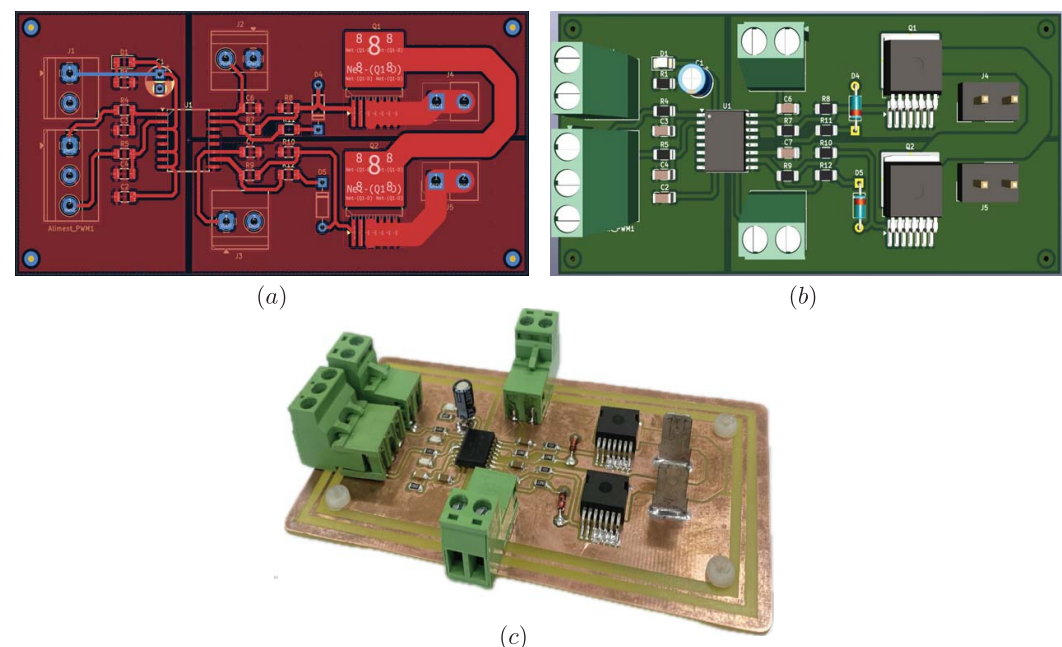
Figure 3b shows the electrical schematic of this stage. It illustrates the anti-series configuration of the two MOSFETs, enabling bidirectional switching. This arrangement is independently controlled by the gate driver's isolated outputs, ensuring that only one device is active during each half-cycle, preventing shoot-through faults. The design of this stage also includes passive protection networks and conditioning elements that help dampen switching oscillations and reduce EMI. Gate resistors were carefully sized to control the rise and fall times of the signals, and the PCB layout was optimized to minimize parasitic inductance between the power terminals.

Table 2. Technical specifications of the IMBG120R053M2H CoolSiC™ 1200 V SiC MOSFET.

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	1200	V
Recommended turn-on gate voltage	$V_{GS(on)}$	15–18	V
On-state drain-source resistance	$R_{DS(on)}$	52.6	m Ω
Maximum junction temperature (overload)	T_{vj}	200	°C
Short-circuit withstand time	t_{SC}	2	μ s
Gate-source threshold voltage	$V_{GS(th)}$	4.2	V

3.3. Printed Circuit Board Design

The PCB was designed to compactly and efficiently integrate both the control and power stages of the bidirectional switch. A single-layer architecture was employed to facilitate manufacturing, reduce production costs, and simplify the assembly process, without compromising the electrical performance of the system. The component layout was carefully planned to minimize the length of critical traces, especially those associated with high-speed switching, in order to reduce parasitic inductance and improve signal integrity. A physical distribution was adopted that clearly separates low- and high-power sections, using independent ground planes and optimized return paths to mitigate electromagnetic interference. Figure 4 shows the final PCB design generated using KiCad software, along with a 3D rendering and final implementation. The general structure of the board can be observed, featuring a symmetrical layout between the two switching channels and extended copper areas to aid thermal dissipation of power devices. Input connectors for power supply and control signals were integrated, as well as robust output terminals for connection to the load stage. The use of SMD technology for nearly all components allowed a high integration density, contributing to the reduction in the module's overall size.

**Figure 4.** PCB design (a) Top layer PCB layout, (b) 3D view and (c) Final assembly of the PCB.

4. Theoretical Analysis

The proposed design has been analyzed in terms of power losses based primarily on switching and conduction losses. Furthermore, for high-voltage switching evaluations of the power transistors, it is essential to have attenuation networks for the voltage surges generated by the load inductances. Therefore, a snubber network has been designed to

attenuate these voltage surges, which could damage the power transistors during the switching process. The electrical schematic of the bidirectional switch with the snubber network can be seen in Figure 5. The suffixes 1 and 2 represent are used to differentiate the power transistor feeds and signals, respectively.

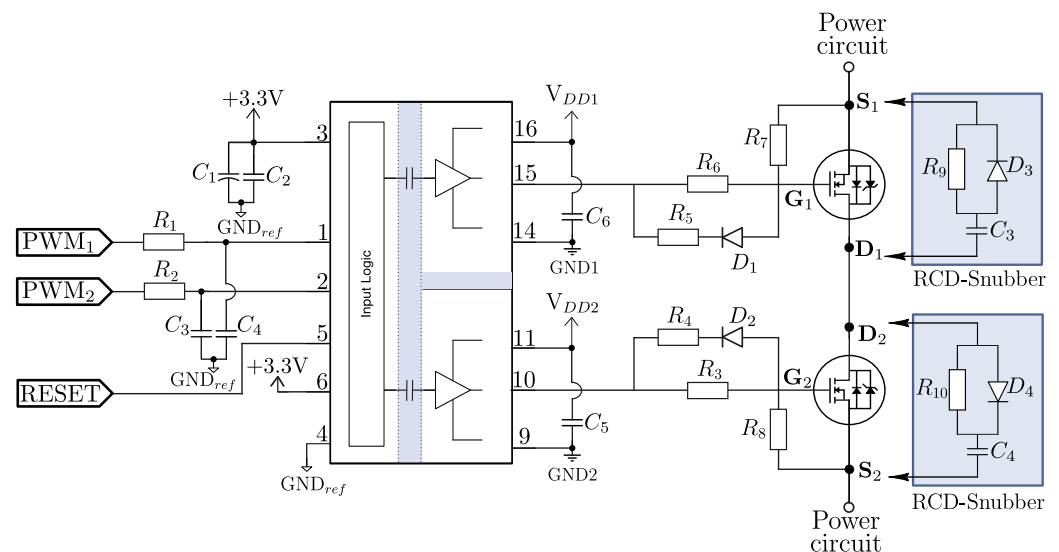


Figure 5. Electrical schematic of the SiC MOSFET gate-drive stage including the RCD snubber network.

4.1. Loss Analysis

Semiconductor switching devices naturally exhibit power losses, for example, due to non-ideal switching of transistors between on and off states. Application-specific operating points are provided in the manufacturer's data sheet [18] and are subject to analysis.

The energy losses E_{ON} and E_{OFF} are given by the equations as follows:

$$E_{ON} = \frac{1}{2} t_{ON} V_{DS} i_L \quad (1)$$

$$E_{OFF} = \frac{1}{2} t_{OFF} V_{DS} i_L \quad (2)$$

where t_{ON} and t_{OFF} are the time it takes to turn on and off, respectively. V_{DS} is the voltage between the Drain and Source terminals and i_L is the maximum current flowing through the SiC-MOSFET. Using the Equations (1) and (2), the switching power losses are calculated, which are given by (3) and (4), where L_{ON} and L_{OFF} are the power losses in the ON and OFF states, respectively, and F_{sw} is the switching frequency.

$$L_{ON} = E_{ON} F_{sw} \quad (3)$$

$$L_{OFF} = E_{OFF} F_{sw} \quad (4)$$

4.2. Snubber Network Calculation

An RCD (resistor-capacitor-diode) snubber network was implemented for the SiC-MOSFET (IMBG120R053M2H), as shown in Figure 5. The purpose of the snubber is to limit the drain–source voltage overshoot generated during turn-off, which results from the interaction between the device's high di/dt and the parasitic inductance of the commutation loop. The work is carried out with a bus voltage of 30 V, a switching frequency of 40 kHz and an estimated turn-off current of 10 A.

The energy stored in the parasitic inductance L_m at the time of shutdown is:

$$E_L = \frac{1}{2} L_m I_{off}^2 \quad (5)$$

This energy is absorbed by the Snubber network capacitor (C_s), resulting in a voltage increase from the bus value V_{DD} to a peak V_{clamp} . Applying energy conservation, we have:

$$\frac{1}{2}L_m I_{off}^2 = \frac{1}{2}C_s(V_{clamp}^2 - V_{DD}^2) \Rightarrow C_s = \frac{L_m I_{off}^2}{V_{clamp}^2 - V_{DD}^2} \quad (6)$$

This equation is presented in [19], investigating the impact of the SiC-MOSFET-Snubber-Diode loop on switching losses.

To prevent energy buildup in the snubber network capacitor, it must be almost completely discharged before the next switching cycle. The recommended time constant is:

$$\tau = R_s C_s \leq \frac{T}{2} \quad (7)$$

This rule of thumb is supported by experimental observations and simulations presented in the studies of [20], where the effect of parasitics on switching performance is analyzed, as well as by [21], which provides a detailed review of switching oscillations.

Considering a Snubber capacitance value $C_s = 10$ nF, a value of $V_{DD} = 30$ V, period $T = 25$ μ s, $I_{off} = 10$ A and $L_m = 15$ nH, along with a calculated value of $E_L = 7.5$ μ J based on (5), the Voltage Clamping (V_{clamp}) at the input is obtained as follows:

$$V_{clamp} = \sqrt{V_{DD}^2 + \frac{2E_L}{C_s}} \approx 48.99 \text{ V}$$

In the case of sizing the discharge resistance value, the analysis in [20] is taken into account, where it is suggested that the time constant of the Snubber network should be less than or equal to half the switching period, that is, $\tau \leq T/2$, to ensure effective discharge of the capacitor. Using this as a basis, we obtain:

$$R_s \leq \frac{\tau}{2C_s} = \frac{12.5 \times 10^{-6}}{10 \times 10^{-9}} = 1250 \Omega$$

5. Results

To validate the operation and performance of the developed bidirectional switch, an experimental platform was designed and built to enable controlled testing under various operating conditions. This experimental phase aims to evaluate the switching behavior in both DC and AC modes, considering variables such as load type, voltage and frequency levels, signal integrity, and associated losses. Figure 6 presents the schematic of the test circuit, which illustrates the electrical connections of the bidirectional switch, the power supply, the gate driver, and the measurement points used for signal observation. This circuit was implemented in practice using the experimental platform shown in Figure 7, which integrates all the necessary elements for powering, applying control signals, and performing measurements in the laboratory environment.

- DC mode: used to assess the individual performance of each switch under controlled conditions with resistive or inductive loads.
- AC mode: intended to evaluate the overall behavior of the Bi-Sw when subjected to alternating signals, simulating real operating conditions such as those encountered in MC.

Throughout the tests, various combinations of voltage and frequency were applied, and real-time measurements were carried out using a digital oscilloscope and differential probes. These measurements enabled observation of waveform shapes, switching losses, transition times, and the dynamic response of the system under different scenarios. This

experimental phase not only confirmed the correct operation of the developed hardware but also provided valuable insights into its behavior in practical direct MC applications.

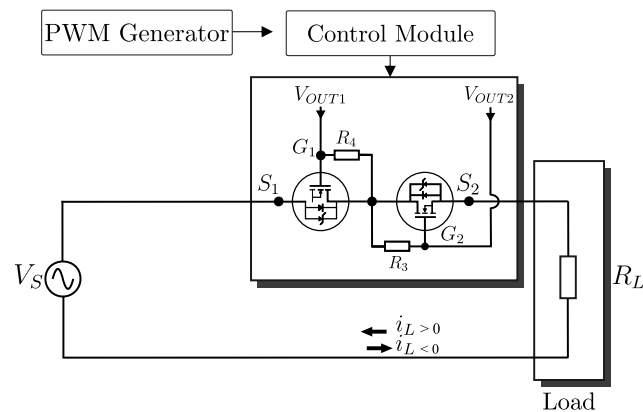


Figure 6. Experimental test circuit diagram.

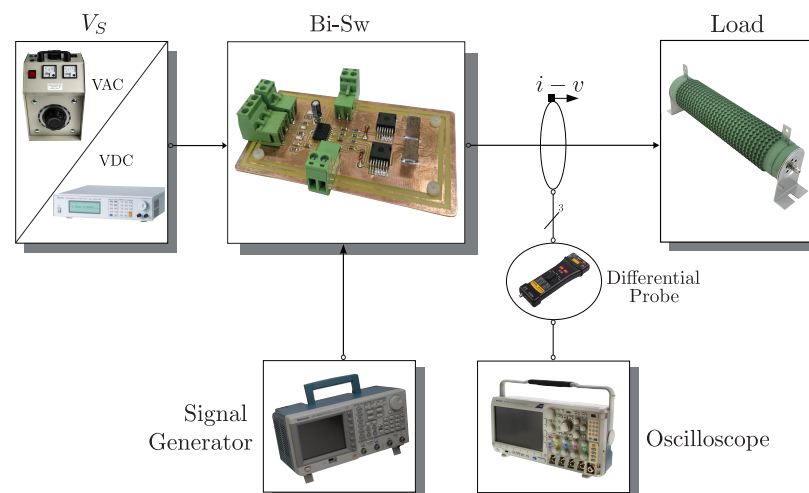


Figure 7. Experimental test bench platform.

5.1. Preliminary Verification of Gate Driver

Before proceeding with the full experimental validation, the operation of the gate driver circuit based on the UCC21521 was verified. A single PWM control signal was applied to both driver inputs simultaneously, enabling the SiC-MOSFETs to switch between cutoff and conduction states. Figure 8 shows the input and output waveforms of the UCC21521 at a switching frequency of 1 kHz. In this figure, the gate-to-source voltage (V_{GS}), the diode voltage, the switch voltage, and the current through the power circuit are shown, confirming that the control signals are properly level-shifted to the gate-drive voltage required for the SiC-MOSFETs.

5.2. Snubber Evaluation

To mitigate the adverse effects of fast switching in SiC-MOSFETs, a snubber circuit was implemented in the power stage. Figure 9 presents the switching waveforms of the bidirectional switch. Figure 9a presents the waveforms of the voltage and current switched by the bidirectional switch without the snubber network, and Figure 9b with the snubber network, under identical operating conditions. In Figure 9a, pronounced overshoots are observed on the falling edge of the signal. These are attributed to the high dv/dt and the circuit's parasitic inductance. Such oscillations can compromise signal integrity and reduce long-term system reliability. In contrast, Figure 9b shows a significant improvement in waveform quality, with reduced amplitude and duration of the oscillations. This confirms

that the snubber effectively damps high-frequency transients, improves switching behavior, and lowers the electrical stress on power devices.

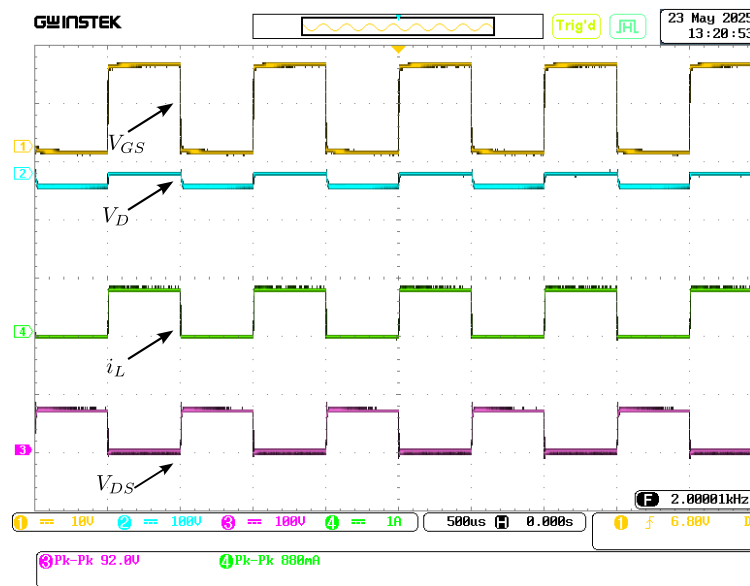


Figure 8. Gate driver input and output waveforms (1 kHz).

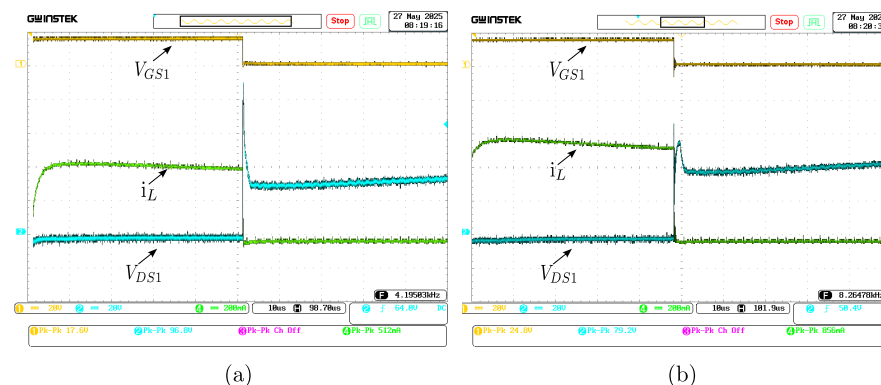


Figure 9. Snubber operation evaluation: (a) without snubber and (b) with snubber.

5.3. Functional Evaluation of the Bidirectional Switch Under AC Operation

To validate the behavior of the bidirectional switch under realistic operating conditions, experimental tests were conducted by varying the input voltage and switching frequency. The initial tests used an AC signal of 50 V, with switching frequencies ranging from 1 kHz to 100 kHz, in 20 kHz increments. The same methodology was subsequently applied to input voltages of 100 V and 150 V, while maintaining the same testing conditions. In all cases, the switch exhibited stable and expected behavior, with clean switching, no triggering failures, and no significant distortions in the output signal—even at high frequencies. These results highlight the effectiveness of the driver design and the robustness of the SiC-MOSFET used, particularly under high-frequency and high-voltage conditions. Figure 10 presents the results for two of the evaluated conditions. Figure 10a shows the system response with a 50 V input, while Figure 10b corresponds to operation with a 150 V input. In both cases, the output waveform is stable and well-defined, confirming the switch's correct operation within the tested range. The signal V_{GS} corresponds to the PWM control signal generated by the control system and applied to the gate driver. The V_S represents the AC voltage applied at the input of the power stage. The V_L is the output

voltage of the switch, reproducing the behavior of the PWM control signal and thereby validating the expected operation.

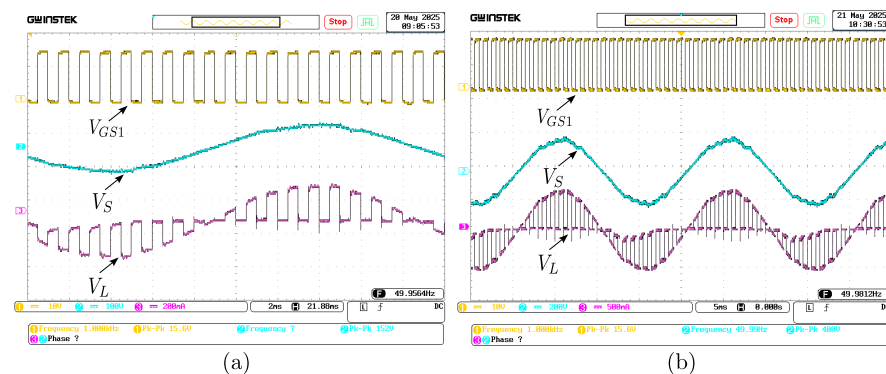


Figure 10. AC operation evaluation: (a) 50 V and (b) 150 V.

5.4. Functional Evaluation of the Bidirectional Switch in DC with 300 Ω Load

To analyze the individual behavior of each switch under forced conduction conditions in DC, the previous tests were replicated using a 300 Ω resistive load. Voltages of 50 V and 100 V were applied, with the PWM control signal frequency ranging from 1 kHz to 100 kHz in 20 kHz increments, while maintaining the same gate-driving strategy.

Figure 11 shows the results for both voltage levels. Figure 11a, on the left, corresponds to the switch operating at 50 V, while Figure 11b, on the right, illustrates its behavior at 100 V. In both waveforms, four key signals are displayed to evaluate the switch performance.

The results show precise, repeatable switching across the evaluated voltage and frequency range. The snubber is shown to function effectively, limiting transient current spikes during turn-off. The voltage waveform is clean and well-defined, with no significant overshoot. The measured current through the switch behaves as expected for a purely resistive load, consistent with the test conditions.

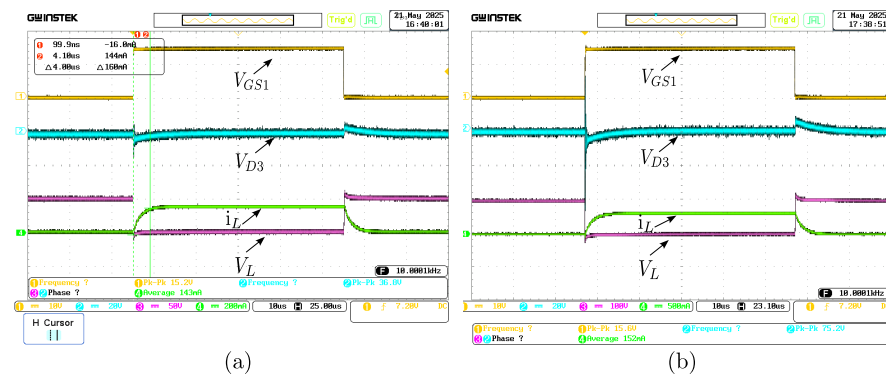


Figure 11. Bi-Sw operation under DC conditions: (a) 50 V and (b) 100 V.

5.5. Functional Evaluation of the Bidirectional Switch in DC with RL Load

The previous tests were replicated using an electric heater as the load, which exhibits an inductive-resistive behavior. Voltages of 50 V and 100 V were applied, and the PWM switching frequency was varied from 1 kHz to 100 kHz in 20 kHz steps. Figure 12 shows the measured signals for two conditions. Figure 12a corresponds to 50 V, and Figure 12b to 100 V. Unlike the purely resistive load case, a more gradual, sustained current waveform is observed due to the inductive effect. The snubber current also shows more pronounced peaks at turn-off, confirming its damping action. In both cases, switching remains stable, with no distortions or significant overshoot.

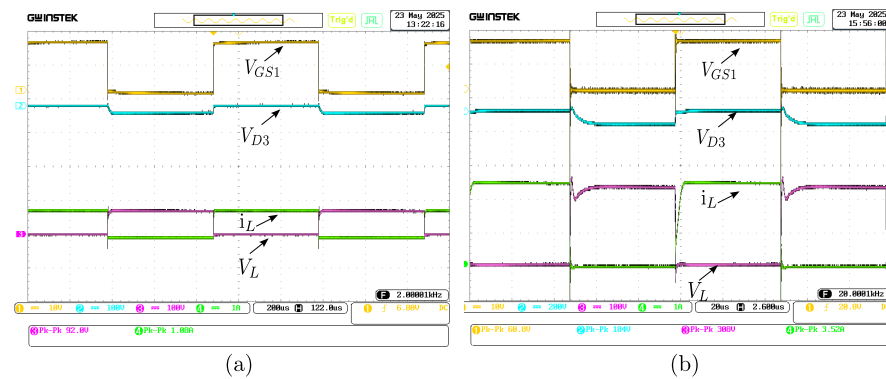


Figure 12. Bi-Sw operation with inductive-resistive load: (a) 50 V and (b) 100 V.

5.6. Experimental Loss Analysis

Based on experimental results across various voltage levels, frequencies, and load types, the switching losses of the bidirectional switch were estimated. To this end, voltage and current waveforms across the switch were analyzed during the turn-on and turn-off transients, allowing the calculation of the energy dissipated in each switching cycle. Figure 13 presents two representative curves derived from the measured data. Figure 13a shows the switching loss as a function of the operating frequency, while Figure 13b displays the accumulated energy dissipated per second of operation. Both curves illustrate the direct impact of increasing the switching frequency on total energy dissipation and serve to validate the efficiency of the proposed design within the evaluated operating range.

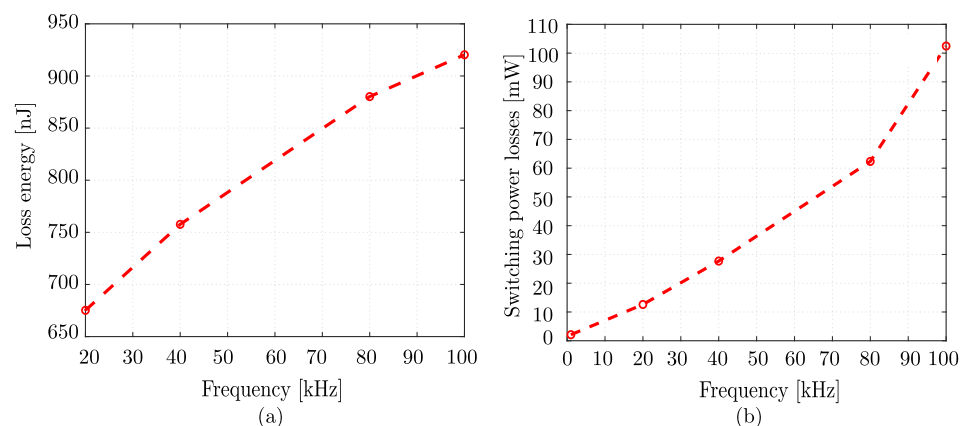


Figure 13. (a) Accumulated energy losses and (b) switching losses of the bidirectional switch with RL load.

6. Conclusions

The design and implementation of the compact Bi-Sw based on SiC-MOSFET technology has demonstrated robust and efficient performance under both DC and AC operating conditions. Experimental tests validated the device's correct switching performance over a wide range of voltages and frequencies, demonstrating low losses, adequate response times, and reliable performance under various load conditions. The results confirm the viability of the proposed design for high-frequency matrix converters, highlighting the usefulness of the modular architecture, SMD integration, and galvanically isolated controllers. Together, these elements enable a scalable, compact solution suitable for future efficiency optimizations and advanced control.

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Abbreviations

The following abbreviations are used in this manuscript:

Bi-Sw	Bidirectional switch
BtB	Back-to-Back converter
DSP	Digital signal processor
EMI	Electromagnetic interferenc
FPGA	Field-Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
MC	Matrix Converter
PEC	Power Electronic Converters
PCB	Printed Circuit Board
SiC-MOSFET	Silicon Carbide Mosfets
SMD	Surface Mount Device
VSI	Voltage Source Inverter

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