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Comparative Analysis of Three- and Five-Level NPC Converters with Predictive Current Control for Reactive Power Compensation: Simulation Study and Experimental Validation of the Three-Level Topology †

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Abstract

This paper presents a comparative analysis of three-level (3L-NPC) and five-level (5L-NPC) Neutral-Point-Clamped converters using Finite Control Set Model Predictive Control (FCS-MPC) for reactive power compensation. The research addresses a critical gap by providing a direct performance comparison under identical operating conditions, supported by simulation and experimental validation of a 3L-NPC prototype. The study evaluates harmonic performance, dynamic response, and DC-link balance. Results demonstrate that the 5L-NPC topology significantly outperforms the 3L-NPC, achieving a simulated grid current Total Harmonic Distortion (THD) of 3.36% compared to 7.84% for the 3L-NPC. This 57.1% reduction in THD allows the 5L-NPC to comply with the IEEE Std. 519-2022 limit (<5%), whereas the 3L-NPC experimental results (9.9% THD) highlight the impact of practical non-idealities such as dead time and sensor noise. While the 5L-NPC offers superior power quality, it entails higher hardware complexity, evaluating 125 switching states compared to 27 in the 3L-NPC. These findings provide quantitative guidelines for selecting NPC topologies in high-performance grid compensation systems.

Keywords: active power filter; finite control set model predictive control; multilevel converters; neutral-point-clamped converter; power quality; reactive power compensation; STATCOM; total harmonic distortion

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1. Introduction

Improving power quality and reactive power management are fundamental requirements in modern electrical systems, particularly in industrial environments and distributed energy networks. Reactive power compensation helps reduce losses, improve voltage profiles, and maintain a high power factor, which are essential for the stability and efficiency of electrical systems [1]. An effective way to achieve this is to use grid-connected power

converters capable of injecting or absorbing reactive power, with exceptional dynamic performance and low harmonic distortion [2]. Among the various power converter topologies, multilevel converters with Neutral Point Clamping (NPC) have emerged as a solution due to their ability to generate stepped voltage waveforms with less distortion and less wear on power semiconductors [3–5]. Specifically, the three-level NPC converter (3L-NPC) is the most widely adopted due to its simple structure and robust operation [6,7], while the five-level NPC converter (5L-NPC) offers higher voltage resolution, allowing for a better approximation of the sine waveform and improved harmonic performance due to the reduction of voltage steps [8,9]. However, this improvement comes at the cost of increased structural complexity. Therefore, selecting between these two topologies involves trade-offs in terms of implementation effort, waveform quality, and control accuracy, particularly when advanced control strategies are employed [10,11].

Several control strategies have been reported for grid-connected power converters dedicated to reactive power compensation. Classical linear approaches, such as proportional–integral (PI) and proportional–resonant (PR) controllers, remain widely adopted due to their simplicity and ease of tuning [12–14]. However, their performance degrades under non-linear load conditions and grid disturbances, and they rely on modulation stages that impose fixed switching frequency constraints [15]. Alternative nonlinear strategies have also been explored. Hysteresis-based control provides fast dynamic response and inherent robustness, albeit at the cost of variable switching frequency and increased harmonic distortion [16]. Sliding mode control (SMC) enhances robustness against parameter uncertainties, but its practical implementation is hindered by chattering and modelling requirements [17].

In this context, Model Predictive Control (MPC), and particularly its Finite Control Set variant (FCS-MPC), has emerged as a suitable alternative for power converter applications [17–19]. By exploiting a system model to predict the future behaviour of the controlled variables, FCS-MPC determines the optimal switching state according to a predefined cost function [18]. This approach enables direct handling of the discrete nature of multilevel converters without requiring a modulation stage, while naturally supporting multi-objective optimisation.

These features make FCS-MPC particularly attractive for reactive power compensation. Specifically, it allows the simultaneous regulation of the output current and the DC-link capacitor voltage balance within a unified control framework, which is essential in NPC-based converters. Moreover, its fast dynamic response provides clear advantages under varying load conditions and grid disturbances [16], and its effectiveness has been extensively validated in NPC applications [16,17,20], establishing a solid benchmark for comparative studies.

However, despite the increasing interest in multilevel NPC topologies, systematic comparisons between three-level (3L-NPC) and five-level (5L-NPC) converters under identical control conditions remain limited. Most existing works focus on the three-level topology [6,7], whereas studies on 5L-NPC converters are typically restricted to efficiency analyses in motor drive applications [8] or lack experimental validation [21].

Furthermore, the specific requirements of reactive power compensation—namely fast dynamic response, low harmonic distortion at the point of common coupling (PCC), and compliance with IEEE Std. 519-2022—have not been jointly assessed for both topologies under FCS-MPC control [16,17,22]. This gap motivates the present work, which provides a direct comparison of 3L-NPC and 5L-NPC converters under identical operating conditions, control strategy, and system parameters.

Despite the growing number of simulation-based studies on NPC converters under FCS-MPC control, works that systematically combine simulation with experimental validation remain limited [7,17].

While simulations are essential for assessing control performance and topology characteristics, they fail to capture several practical non-idealities, including switching dead time, gate driver dynamics, parasitic impedances, and constraints associated with real-time digital implementation [19]. As a result, discrepancies between simulated and experimental performance are typically observed, often manifested as increased current distortion in practical implementations [23].

Therefore, experimental validation is essential to assess the practical performance of the proposed approach. In this work, such validation is carried out on the three-level NPC converter, while the five-level topology is analysed through simulation under equivalent operating conditions, enabling a consistent and meaningful comparison [15]. This study addresses this gap by incorporating experimental validation of a 3L-NPC converter prototype operating under an FCS-MPC current control strategy for reactive power compensation [24,25]. Measured performance indicators, including THD and power factor, are compared with simulation results to assess the impact of practical hardware constraints and implementation effects. In addition, the 5L-NPC topology is analyzed via simulation to estimate the potential performance improvements achievable by increasing the voltage resolution of the converter [26,27]. Although the 5L-NPC converter is not experimentally validated in this work, its performance is evaluated under the same operating conditions, control strategy, and system parameters as the experimentally validated three-level prototype. This ensures a consistent and fair comparative framework, enabling reliable assessment of the relative performance improvements associated with higher voltage levels. The main contributions of this work can be summarized as follows:

- First direct systematic comparison of 3L-NPC and 5L-NPC converters under identical FCS-MPC conditions, filter parameters, and operating conditions for reactive power compensation, a scenario not previously addressed in the literature [6–8,21].
- Experimental validation of a 3L-NPC prototype under FCS-MPC for reactive power compensation, with quantification of the simulation-to-experiment discrepancy in THD (25%) and DC-link voltage imbalance (56%), attributed to specific hardware non-idealities including IGBT dead time, gate driver propagation delays, and sensor noise.
- Evaluation of IEEE Std. 519-2022 compliance for both topologies under FCS-MPC [22], providing quantitative design guidelines for topology selection in grid-connected reactive power compensation systems.
- Design and validation of a replicable instrumentation framework based on custom sensor boards incorporating the CS60-100L current transformer and AMC1350 galvanically isolated amplifier for FCS-MPC experimental platforms.

The remainder of this paper is organized as follows. Section 2 describes the proposed compensation system, the mathematical model, and the predictive current control strategy. Section 3 presents the obtained results, including the experimental setup, simulation results, and experimental validation. Section 4 provides a comparative discussion of the obtained results, and Section 5 concludes the paper.

2. Description of the Proposed System

The compensation system consists of an NPC converter connected in parallel to a three-phase inductive load and the electrical grid, as shown in Figure 1. The balanced three-phase network supplies a load that requires both active and reactive current components. To model the effects of the transmission line, series inductances are included to represent the network impedance. The NPC converter acts as an active compensator by injecting or absorbing reactive current, thereby improving the power factor at the PCC [28,29]. The proposal addresses the 3L-NPC and 5L-NPC converters, shown in Figure 2a,b, respectively.

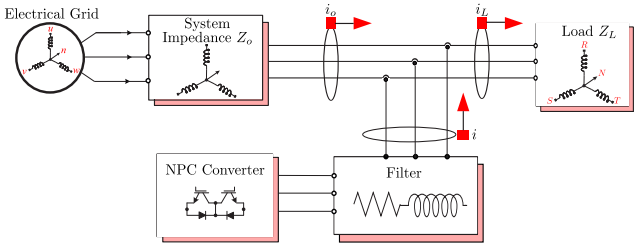
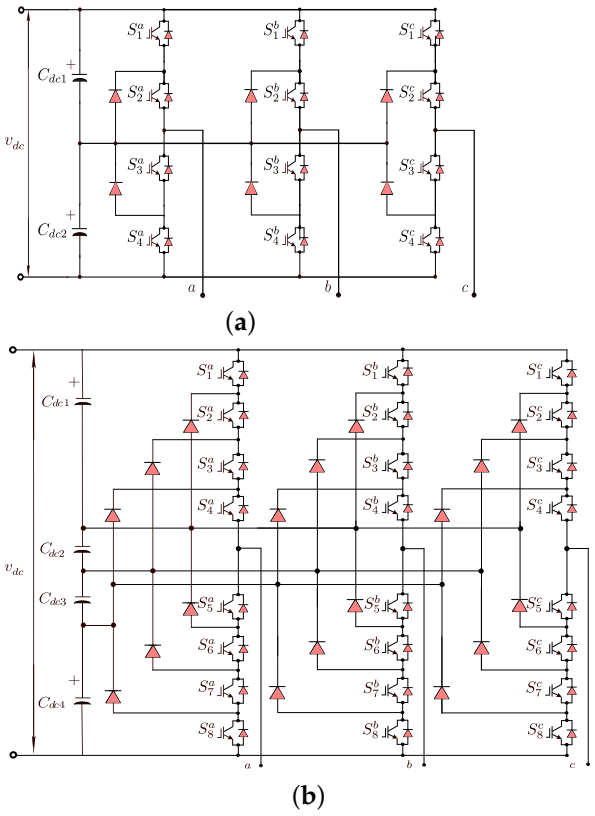


Figure 1. NPC-based shunt compensation system connected to the electrical grid and load through an output filter, where reactive current is injected at the point of common coupling. The system involves three main current components: the current injected by the converter through the output RL filter (i), the grid current (i_o), and the load current (i_L). These currents correspond to the per-phase variables i_x, $i_{o,x}$, and $i_{L,x}$, respectively, with $x \in \{a, b, c\}$, as formally defined in the mathematical model presented in Section 2.



(**a**)

(**b**)

Figure 2. NPC converter topologies considered in this work: (**a**) 3L-NPC; (**b**) 5L-NPC.

The adopted control strategy is predictive and designed to accurately follow the reference current. In addition, a passive RL filter is incorporated between the converter and the grid to attenuate high-frequency switching harmonics and smooth the injected current waveform [30].

2.1. Mathematical Model of the Control System for NPC Converters

The FCS-MPC control strategy for reactive power compensation via current control requires two fundamental components: a plant dynamic model and a current reference to track. The reference is calculated based on instantaneous power theory, which allows the active and reactive components of the load to be separated. On the other hand, the plant model is obtained from the RL-type passive filter connected to the converter output, which determines the dynamics of the current injected into the system [31]. To this end, the three-phase voltage signals $\mathbf{v}_{abc}$ and current signals $\mathbf{i}_{abc}$ are transformed to the $\alpha\beta 0$

reference frame using the power-invariant Clarke transformation [32], represented by the matrix **T**.

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1}$$

$$\mathbf{X}_{\alpha\beta 0} = \mathbf{T} \cdot \mathbf{X}_{abc}$$

where **T** is the Clarke transformation matrix invariant with power, $\mathbf{X}_{abc}$ represents the three-phase quantity in the natural frame (voltage or current), and $\mathbf{X}_{\alpha\beta 0}$ denotes the transformed quantity in the stationary reference frame $\alpha\beta 0$. With the transformed voltages and currents, the instantaneous active (P) and reactive (Q) power are calculated:

$$P = v_\alpha i_\alpha + v_\beta i_\beta \tag{2}$$

$$Q = v_\beta i_\alpha - v_\alpha i_\beta \tag{3}$$

where v_α and v_β are the grid voltage components, i_α and i_β are the current components in the $\alpha\beta$ reference frame, P is the instantaneous active power, and Q is the instantaneous reactive power. The reference current $\mathbf{I}^*_{\alpha\beta 0}$ is calculated by setting the reference active power to zero and inverting the reactive power value.

$$\mathbf{I}^*_{\alpha\beta 0} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ -Q \end{bmatrix} \tag{4}$$

where v_α and v_β are the voltage components in the $\alpha\beta$ reference frame, Q is the instantaneous reactive power to be compensated, and the active power reference is set to zero to achieve pure reactive power compensation. The term $v_\alpha^2 + v_\beta^2$ represents the squared magnitude of the grid voltage vector, which normalizes the reference current amplitude with respect to the grid voltage level. The reference current is transformed into the *abc*-frame for comparison with the controller's predictions [33].

$$\mathbf{I}^*_{abc} = \mathbf{T}^{-1} \left[\mathbf{I}^*_{\alpha\beta 0} \right] \tag{5}$$

where $\mathbf{T}^{-1}$ is the inverse Clarke transformation matrix and $\mathbf{I}^*_{\alpha\beta 0}$ is the reference current vector in the stationary $\alpha\beta 0$ reference frame. The reference current generation procedure is identical for both the 3L-NPC and 5L-NPC topologies, since it depends exclusively on the measured grid voltages and load currents, and is independent of the number of converter voltage levels. Specifically, the three-phase load currents and grid voltages are measured and transformed to the $\alpha\beta 0$ frame via the power-invariant Clarke transform (1). The instantaneous active and reactive powers are then computed using (2) and (3), and the reference current $\mathbf{I}^*_{\alpha\beta 0}$ is obtained by setting the active power reference to zero and inverting the reactive power (4). Finally, the reference is transformed back to the *abc* frame via the inverse Clarke transform for direct use in the FCS-MPC cost function (8).

2.2. Predictive Current Control Strategy for Multilevel NPC Converters

The FCS-MPC controller is designed based on the discrete-time dynamic model of the RL output filter, which governs the current injected into the grid. The continuous-time dynamics of the filter current are described by:

$$L_c \frac{di_x}{dt} = v_x - R_c i_x - v_{c_k} \tag{6}$$

where v_x is the grid phase voltage, i_x is the filter current, v_{c_k} is the converter output voltage determined by the active switching state, and R_c, L_c are the filter resistance and inductance, respectively. Applying the first-order Euler forward discretization with sampling period T_s, the discrete-time prediction model is obtained as given in as given in (7). The controller bandwidth is determined by the filter parameters and the sampling period: with $L_c = 10$ mH, $R_c = 0.3\ \Omega$, and $T_s = 10$ µs, the filter time constant is $\tau = L_c/R_c = 33.3$ ms, which is significantly larger than the sampling period, ensuring that the discrete model accurately represents the continuous-time dynamics and that the predictive controller can track the reference current within each sampling interval. The same controller design and plant model are applied identically to both the 3L-NPC and 5L-NPC topologies; the only difference between the two cases is the set of admissible switching vectors evaluated at each sampling instant (27 for the 3L-NPC and 125 for the 5L-NPC). In multilevel converters, the number of levels and phases determines the number of possible switching states. Thus, in a 3L-NPC converter, there are 27 possible states, whereas in a 5L-NPC converter, there are 125 possible states [20]. The flowchart of the control scheme is shown in Figure 3.

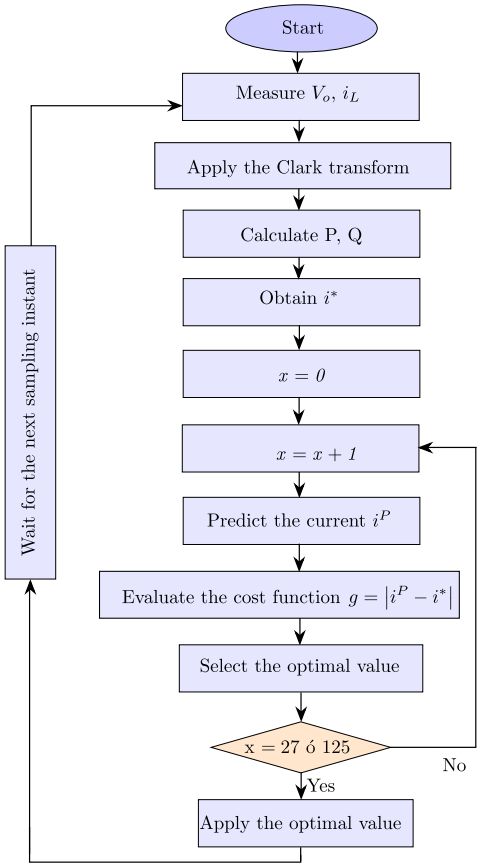


Figure 3. Flowchart of the proposed finite control set model predictive control (FCS-MPC) strategy for current regulation.

For each possible switching state, the current predicted by the discrete model (i_x^p) is evaluated based on the current and voltage across the filter (i_x, v_x) at the current instant:

$$i_x^p = \left(1 - \frac{T_s R_c}{L_c}\right) i_x + \frac{T_s}{L_c}\left(v_x - v_{c_k}\right) \tag{7}$$

In this expression, i_x and v_x are the measured phase current and grid voltage at the current time step, where $x \in \{a, b, c\}$, T_s is the sampling time, R_c and L_c represent the filter parameters, and v_{c_k} is the voltage applied to the converter output according to the switching state [34]. The selection of the optimal state is performed by minimizing a cost function:

$$g = \sum_{x \in \{a,b,c\}} (i_x^* - i_x^p)^2 + \lambda \Delta V_c \quad (8)$$

where i_x^* is the reference current for phase $x \in \{a, b, c\}$, i_x^p is the predicted current for the same phase, λ is the weighting factor that balances current tracking accuracy against DC-link voltage balance, and ΔV_c is the voltage imbalance between the DC-link capacitors. The cost function g is evaluated jointly for all three phases simultaneously for each of the N admissible switching vectors $\mathbf{S}_k = (S_a, S_b, S_c)$, where each component takes integer values within the set of available voltage levels. The optimal switching vector $\mathbf{S}^*$ is the one that minimizes g over all admissible combinations, and is applied to the converter at the next sampling instant. The optimal switching vector $\mathbf{S}^* = (S_a, S_b, S_c)$ selected by minimizing the cost function (8) is directly applied to the converter at the next sampling instant, without requiring a separate modulation stage. The gate signals corresponding to $\mathbf{S}^*$ are generated by the dSPACE MicroLabBox real-time platform and routed through dedicated gate driver boards to the IGBT switches (SEMIKRON SKM50GB12T4) of each converter leg, ensuring that the commanded switching state is physically realized within the sampling period $T_s = 10$ µs.

This scheme evaluates phases a, b, and c individually and selects the optimal switching vector that minimizes the cost function gx [20]. The second term of the cost function, $\lambda \Delta V_c$, introduces a penalty mechanism proportional to the voltage imbalance between the DC-link capacitors. In 3L-NPC and 5L-NPC converters, it is essential to keep the voltages of the intermediate capacitors balanced to avoid distortions in the output waveform, device saturation, and degradation of overall system performance [17]. The parameter λ allows the relative importance of voltage balance to be weighted against current tracking, thereby adjusting the priority between waveform quality and internal converter stability [16,19]. Regarding the stability of the proposed FCS-MPC strategy, it is important to note that FCS-MPC does not rely on a closed-form stability proof in the classical Lyapunov sense; instead, its stability properties are established through the bounded nature of the cost function and the finite prediction horizon. At each sampling instant, the algorithm selects the switching state that minimizes the current tracking error, ensuring that the predicted current converges toward the reference trajectory. The inherent boundedness of the cost function g (8) combined with the discrete nature of the admissible switching states, guarantees that the tracking error remains bounded under nominal operating conditions [16,17]. Furthermore, the DC-link voltage balance term $\lambda \Delta V_c$ in the cost function acts as a stabilizing penalty that actively prevents capacitor voltage divergence. The experimental results presented in Section 3 confirm the practical stability of the implementation, evidenced by the bounded steady-state THD, near-unity power factor, and stable DC-link voltage balance achieved under the proposed control strategy.

2.3. Selection of the Weighting Factor λ

The weighting factor λ in the cost function (8) determines the relative priority between the current tracking accuracy and DC-link capacitor voltage balance. Since these two terms are expressed in different physical unitssquared amperes and volts, respectively—λ must be tuned to normalize their contributions and ensure that neither objective dominates the other inappropriately.

In this study, λ was selected empirically through an iterative simulation-based procedure. For each candidate value, the steady-state grid current THD and the peak DC-link voltage imbalance ΔV_c were recorded under nominal operating conditions. The value $\lambda = 0.05$ was found to provide the best compromise between current waveform quality and capacitor voltage regulation for both the 3L-NPC and 5L-NPC topologies, and was

adopted in all simulations and experimental tests reported in this work. Lower values of λ yielded improved current tracking at the expense of increased voltage imbalance, while higher values improved capacitor balancing but degraded THD performance, consistent with the trade-off behavior reported in the literature [13,14].

It should be noted that the optimal value of λ is system-dependent and may require readjustment when the filter parameters, DC-link capacitance, or operating point change significantly. The development of systematic or model-based methods for selecting weighting factors in FCS-MPC remains an active research topic and is identified as a direction for future work.

Table 1 summarizes the steady-state grid current THD and peak DC-link voltage imbalance ΔV_c obtained for five candidate values of λ under nominal operating conditions. The results confirm the expected trade-off behavior: as λ decreases from 0.20 to 0.01, the grid current THD reduces from 9.91% to 6.92%, reflecting improved current tracking accuracy, while the DC-link voltage imbalance ΔV_c increases from 0.51 V to 4.21 V, indicating degraded capacitor voltage regulation. Conversely, higher values of λ prioritize voltage balance at the expense of increased harmonic distortion. The value $\lambda = 0.05$ was selected as it achieves a THD of 7.84% while maintaining $\Delta V_c = 1.92$ V, representing the best compromise between both objectives under the given operating conditions. This value was therefore adopted for all simulations and experimental tests reported in this work.

Table 1. Effect of the weighting factor λ on grid current THD and DC-link voltage imbalance ΔV_c for the 3L-NPC converter under nominal operating conditions.

λ	THD (%)	ΔV_c (V)
0.01	6.92	4.21
0.02	7.10	3.85
0.05	7.84	1.92
0.10	8.63	0.98
0.20	9.91	0.51

3. Obtained Results

3.1. Experimental Setup: Laboratory Prototype of the 3L-NPC Converter

The experimental prototype of the 3L-NPC converter was constructed using SEMIKRON SKM50GB12T4 IGBT modules. To ensure a realistic evaluation of the system's performance and to support the efficiency and thermal analysis conducted in this study, the critical electrical and thermal parameters of these semiconductor devices are summarized in Table 2.

Table 2. Critical parameters of the SEMIKRON SKM50GB12T4 IGBT module.

Parameter	Symbol	Value
Collector–emitter voltage	V_{CES}	1200 V
Continuous collector current ($T_c = 80$ °C)	I_C	50 A
Collector–emitter saturation voltage ($I_C = 50$ A, $T_j = 25$ °C)	$V_{CE(sat)}$	1.85 V
Turn-on switching energy (per pulse)	E_{on}	4.3 mJ
Turn-off switching energy (per pulse)	E_{off}	5.5 mJ
Thermal resistance (junction to case)	$R_{th(j-c)}$	0.53 K/W

Experimental validation was carried out using a 3L-NPC converter prototype assembled at the Center for Research in Hydroelectric Technologies and Distributed Energy (CITHED), Faculty of Engineering, Universidad Nacional de Asunción (FIUNA), Paraguay. The DC-link was supplied by a regulated DC power source configured at 50 V and 8 A, providing a stable bus voltage for converter operation. The three-phase inductive load

connected to the output consisted of 7.5 Ω resistors and 10 mH inductors per phase, configured as an isolated balanced RL load to emulate a reactive power demand representative of industrial conditions [35]. The complete experimental test bench is shown in Figure 4. The predictive current control algorithm was implemented on a dSPACE MicroLabBox real-time platform, which provides a high-performance FPGA and dual-core processor architecture suitable for demanding control tasks such as FCS-MPC. The MicroLabBox enabled execution of the predictive algorithm within the required sampling period, with all 27 switching state evaluations performed in real time at each control cycle, in accordance with the expression $N = L^3$ described in Section 2.2. The gate signals generated by the control platform were routed through dedicated gate driver boards to the IGBT switches of the converter legs, and the optimal switching vector selected by minimizing the cost function g_x was applied at each sampling instant.

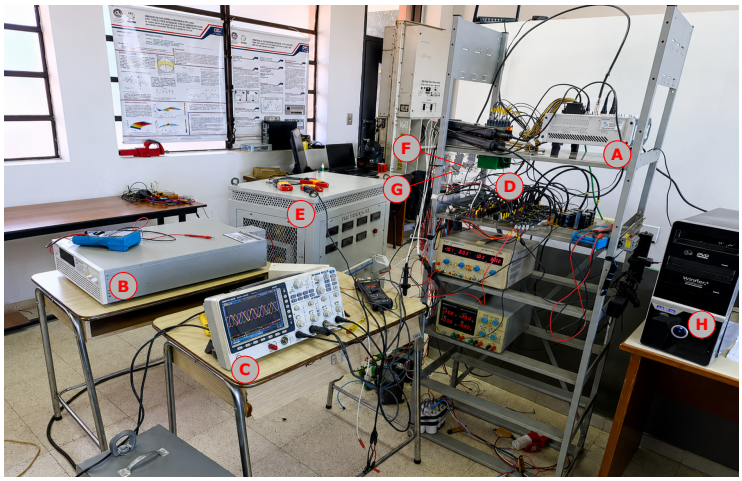


Figure 4. Experimental test bench of the 3L-NPC converter. The main components are identified as follows: (**A**) dSPACE MicroLabBox real-time control platform; (**B**) regulated DC power supply (50 V, 8 A); (**C**) digital oscilloscope (GW Instek, New Taipei City, Taiwan); (**D**) 3L-NPC converter prototype with IGBT modules and gate driver boards; (**E**) three-phase inductive load ($R_l = 7.5\ \Omega$, $L_l = 10$ mH per phase); (**F**) custom current sensor board (CS60-100L, Coilcraft); (**G**) custom voltage sensor board (AMC1350, Texas Instruments); (**H**) PC workstation running MATLAB/Simulink for control algorithm deployment and data acquisition.

3.2. Measurement System

Current measurements were performed using a custom-designed board based on the CS60-100L current transformer (Coilcraft, Cary, IL, USA), a linear integrated sensor capable of measuring AC and DC currents up to 100 A. The secondary current is converted into a voltage signal by a 220 Ω shunt resistor, which is then conditioned by a galvanically isolated AMC1350 instrumentation amplifier (Texas Instruments, Dallas, TX, USA) providing up to 5 kV_{RMS} isolation.

A two-stage amplification circuit based on the OPA2227 operational amplifier yields a differential output in the ±10 V range, compatible with the dSPACE MicroLabBox analog input channels. Voltage measurements at the PCC were obtained using a dedicated board incorporating a resistive voltage divider scaled for up to 380 V_{RMS}, followed by the same AMC1350 isolated amplifier stage and a secondary conditioning circuit based on OPA27 and OPA350 operational amplifiers, providing dual outputs of ±10 V and 0–3 V to support both the dSPACE platform and DSP-based controllers. Both sensor boards incorporate galvanically isolated DC-DC power supplies (IH0512S) to ensure full electrical isolation between the power and control stages, improving immunity to electromagnetic interference generated by the converter switching. An anti-aliasing RC filter with a cutoff frequency

of 48.2 kHz was implemented at the AMC1350 output in both sensor circuits. All sensors were calibrated prior to the experimental campaign to minimize offset and gain errors. The measurement components were selected based on specific technical criteria relevant to the switching converter environment. The CS60-100L current transformer (Coilcraft, Cary, IL, USA) was chosen for its wide measurement range (up to 100 A), linear response, and compatibility with the ±10 V analog input range of the dSPACE MicroLabBox. The AMC1350 instrumentation amplifier (Texas Instruments, Dallas, TX, USA) was selected for its galvanic isolation capability (up to 5 kV_{RMS}), low offset error, and high common-mode rejection ratio, which are critical in switching environments where electromagnetic interference is significant. The dSPACE MicroLabBox was adopted as the real-time control platform due to its dual-core processor and FPGA architecture, enabling real-time execution of the FCS-MPC algorithm and evaluation of all 27 switching states within the required $T_s = 10$ µs sampling period. While alternative components of equivalent or superior specifications could be employed, the dominant sources of THD degradation identified in this work—namely IGBT dead time and gate driver propagation delays—are inherent to the power stage and would not be significantly mitigated by sensor substitution alone. The selected instrumentation therefore represents a suitable and well-validated framework for assessing FCS-MPC performance under practical operating conditions.

3.3. Remarks on Parameter Differences Between Simulation and Experiment

It is acknowledged that the system parameters used in the simulation and experimental validation differ in several key values, as summarized in Table 3. Specifically, the DC-link voltage was set to $V_{dc} = 400$ V in simulation and reduced to $V_{dc} = 50$ V in the experimental prototype, while the load resistance and inductance were adjusted from $R_l = 40\ \Omega$, $L_l = 114$ mH to $R_l = 7.5\ \Omega$, $L_l = 10$ mH, respectively. These differences arise from practical laboratory constraints, including the voltage and current ratings of the available IGBT modules, gate driver boards, and DC power supply, which limited the operating voltage of the prototype to a reduced-scale level. Despite these differences, the comparative validity of the study is preserved for the following reasons. First, the filter parameters (R_c, L_c) and the sampling period (T_s) are identical in both scenarios, ensuring that the current control dynamics governed by the FCS-MPC algorithm operate under equivalent conditions. Second, the per-unit behavior of the predictive controller is largely independent of the absolute voltage scale, since the cost function minimization in (8) depends on current tracking error rather than on absolute power levels. Third, the primary objective of the experimental validation is to quantify the impact of hardware non-idealities—such as IGBT dead time, gate driver delays, and sensor noise—on THD performance, rather than to replicate the exact power levels of the simulation scenario. The reduced-scale prototype is therefore considered a valid platform for assessing implementation effects under the proposed control strategy. The fabricated PCB prototypes and the experimental validation setup are shown in Figure 5.

Table 3. System Parameters Used in Simulation and Experimental Validation.

Parameter	Symbol	Simulation	Experimental
DC-link voltage	V_{dc}	400 V	30 V
DC-link current	I_{dc}	2 A	8 A
DC-link capacitance	C	4700 µF	4700 µF
Filter resistance	R_c	0.3 Ω	0.3 Ω
Filter inductance	L_c	10 mH	10 mH
Load resistance	R_l	40 Ω	7.5 Ω
Load inductance	L_l	114 mH	10 mH
Sampling period	T_s	10 µs	10 µs

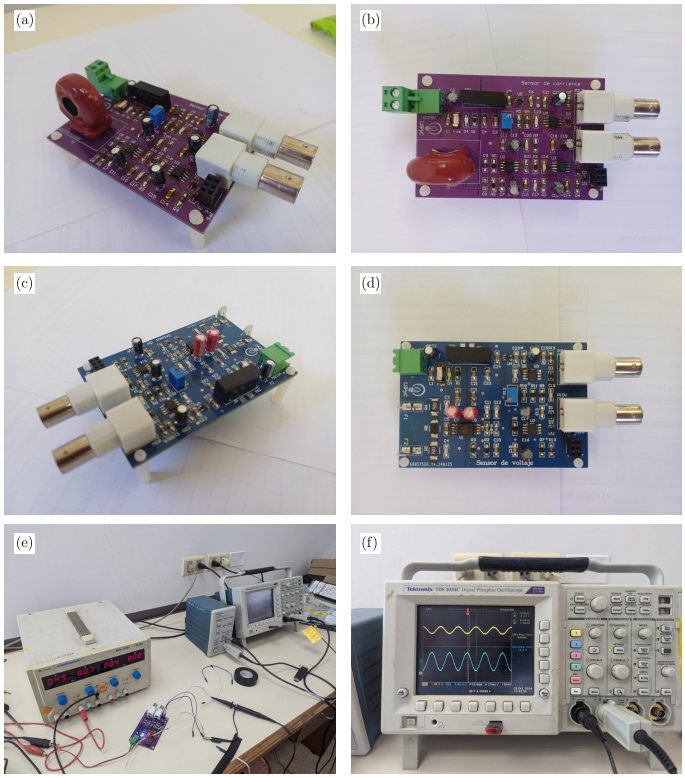


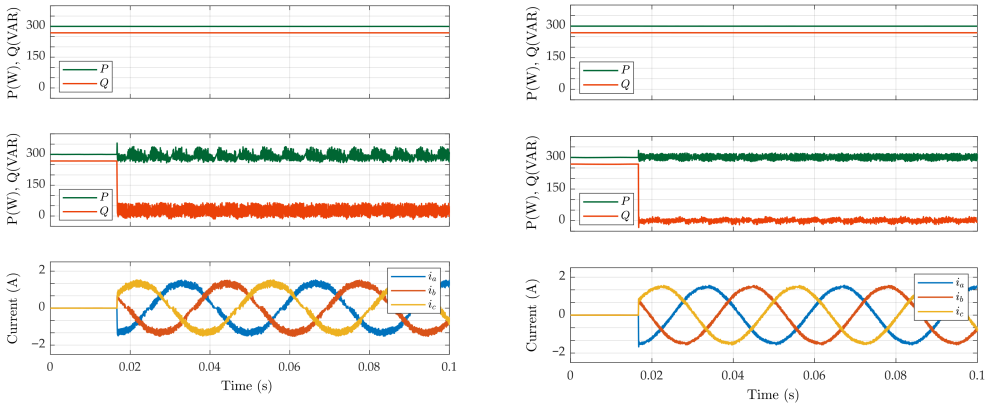
Figure 5. Experimental setup and sensor hardware used for system validation: (**a**,**b**) current sensor PCB (CS60-100L); (**c**,**d**) voltage sensor PCB (AMC1350); (**e**,**f**) laboratory test bench.

3.4. Simulation Results

The MATLAB/Simulink 2024a environment was used to evaluate and compare the performance of the 3L-NPC and 5L-NPC converters under identical operating conditions, with FCS-MPC applied to reactive power compensation in a three-phase inductive load prior to experimental validation. Figure 6 illustrates the temporal evolution of the active and reactive power consumed by the load, the power observed at the grid, and the current injected by the converter. In both cases, the reactive component of the load is effectively canceled, resulting in an almost constant active power profile at the grid and a properly synchronized compensating current. The 5L-NPC converter exhibits a smoother current waveform with reduced ripple, indicating improved tracking of the reference current [36]. Figure 7 shows the grid current waveform and its spectral analysis based on THD calculation. The 3L-NPC converter achieves a THD of 7.84%, while the 5L-NPC reduces this value to 3.36%, representing a significant improvement in the quality of the injected current. This reduction in harmonic distortion is attributed to the higher voltage resolution of the 5L-NPC converter, which enables a more accurate approximation of the sinusoidal

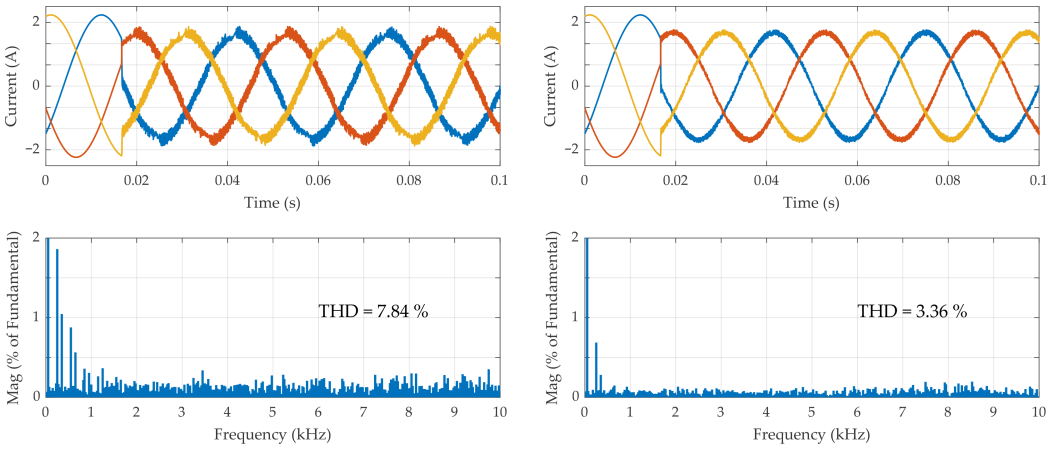
waveform. These results validate the effectiveness of the proposed control strategy for both converters and highlight the superior harmonic performance of the 5L-NPC topology.

Regarding DC-link capacitor voltage balance, the penalty term $\lambda \Delta V_c$ in the cost function regulated the voltage distribution across the DC-link capacitors in both topologies. For the 3L-NPC converter with $\lambda = 0.05$, the steady-state peak imbalance was $\Delta V_c = 1.92$ V, corresponding to 0.48% of the total DC-link voltage ($V_{dc} = 400$ V), as reported in Table 1. This confirms that the balancing objective is achieved without significantly compromising current tracking quality under the selected weighting factor. For the 5L-NPC converter, which requires regulating four series capacitors at $V_{dc}/4 = 100$ V each, the balance error is defined as the voltage difference between the upper capacitor pair $(V_{C1} + V_{C2})$ and the lower pair $(V_{C3} + V_{C4})$. The cost function penalty term was verified to maintain the capacitor voltages within an acceptable range under the simulated operating conditions, consistent with the balancing performance reported for the 3L-NPC topology in Table 1.



(**a**) (**b**)

Figure 6. Reactive power compensation results for NPC converters: (**a**) 3L-NPC; (**b**) 5L-NPC. From top to bottom: active and reactive power consumed by the load, active and reactive power observed at the grid, and inverter output currents.



(**a**) (**b**)

Figure 7. Grid current waveforms and harmonic distortion for NPC converters: (**a**) 3L-NPC; (**b**) 5L-NPC. Top: three-phase grid currents. Bottom: frequency spectrum and THD.

3.4.1. Effective Switching Frequency

Unlike carrier-based modulation schemes, FCS-MPC does not impose a fixed switching frequency; instead, the switching events are determined at each sampling instant by the cost function minimization process. As a result, the effective switching frequency varies with the operating point, the reference current trajectory, and the weighting factor λ.

In this study, the sampling period was set to $T_s = 10$ µs for both topologies, corresponding to a maximum theoretical switching frequency of $f_{sw,max} = 1/T_s = 100$ kHz. However, because the optimal switching state selected at each instant need not differ from the previous one, the average effective switching frequency is considerably lower in practice. For the 3L-NPC converter, the average switching frequency observed in simulation was approximately $f_{sw,avg} \approx 10$ kHz, consistent with the harmonic distribution observed in the THD spectrum of Figure 7, where harmonic energy is concentrated around this frequency band. The experimental prototype exhibited a similar average switching frequency, as evidenced by the comparable harmonic profile of the measured grid current. For the 5L-NPC topology, the finer voltage quantization available with five output levels reduces the magnitude of each current correction step, resulting in a lower average switching frequency for equivalent current-tracking accuracy, thereby contributing directly to the reduced THD of 3.36% reported in simulation.

3.4.2. Simulation Model Validation

The credibility of the MATLAB/Simulink simulation model is established through its correspondence with the experimental results obtained for the 3L-NPC prototype. The discrete-time plant model used in the FCS-MPC algorithm, given by (7), is derived analytically from the first-order Euler discretization of the RL filter dynamics, ensuring that the simulation accurately represents the current prediction mechanism implemented on the dSPACE MicroLabBox platform. Quantitative validation is provided by the comparison presented in Table 5: the simulated grid current THD of 7.84% and the experimental value of approximately 9.9% yield a discrepancy of 25%, which is fully attributable to hardware non-idealities not represented in the ideal simulation environment, including IGBT dead time, gate driver propagation delays, and sensor noise. The remaining performance indicators—power factor, dynamic response, and reactive power compensation effectiveness—show consistent agreement between simulation and experiment, as summarized above. This correspondence confirms that the simulation model faithfully captures the dominant dynamics of the system and provides a reliable basis for evaluating the 5L-NPC topology under equivalent conditions.

3.5. Experimental Results

3.5.1. Experimental Reactive Power Compensation

The experimental test confirmed that the 3L-NPC converter operating under FCS-MPC can provide real-time reactive power compensation. The key quantitative performance indicators obtained during the experimental validation are summarized in Table 4.

The Appendix A provides additional details of the experimental setup and simulation parameters used in the study.

Table 4. Experimental reactive power compensation performance of the 3L-NPC converter ($V_{dc} = 50$ V, $R_l = 7.5\ \Omega$, $L_l = 10$ mH, $T_s = 10$ µs).

Parameter	Before Compensation	After Compensation
Reactive power at PCC, Q (VAR)	≈119	≈0
Active power at PCC, P (W)	≈284	≈284
Power factor at PCC	≈0.92	≈1.0
Settling time, t_{ss} (ms)	—	≈10
Peak compensating current (A)	—	≈8

Upon activation of the compensator, the converter supplied the reactive current component demanded by the inductive load, reducing the reactive power drawn from the

grid from approximately 119 VAR to near zero in a steady state, as summarized in Table 4. The power factor at the PCC improved from approximately 0.92—characteristic of the uncompensated RL load ($R_l = 7.5\ \Omega$, $L_l = 10$ mH at 50 Hz)—to near unity (≈1.0) upon compensator activation. These results are consistent with the waveforms captured in Figure 8, which shows the three-phase load currents transitioning from a lagging power factor condition to an in-phase profile.

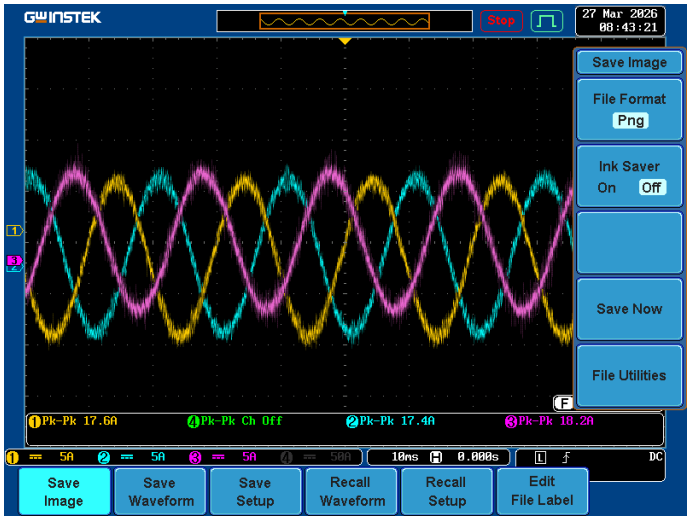


Figure 8. Oscilloscope capture of the three-phase load currents in the 3L-NPC converter system.

The three-phase compensating current injected by the converter tracked the calculated reference with a settling time of approximately $t_{ss} \approx 10$ ms, measured from compensator activation to the achievement of steady-state compensation, with no observable overshoot in the reactive current trajectory. This fast transient response is consistent with the single-step prediction horizon inherent to FCS-MPC, which enables direct selection of the optimal switching state at each sampling instant [17]. The slight increase in settling time relative to the simulated value of $t_{ss} \approx 8$ ms is attributable to gate driver propagation delays and the finite rise time of the IGBT switches.

3.5.2. Experimental THD Measurement

The FFT analysis of the measured grid current yielded a THD of 9.9%, exceeding both the simulated value of 7.84% and the 5% limit defined by IEEE Std. 519-2022. Figure 9 presents this result. This deviation is primarily due to practical non-idealities not captured in the idealized simulation model. Specifically, the insertion of IGBT dead-time intervals to prevent shoot-through introduces output voltage distortion that degrades current waveform quality; finite gate driver propagation delays during turn-on and turn-off events cause misalignment between commanded and actual switching instants, increasing harmonic content; noise present in the current and voltage sensing chains corrupts the feedback signals and reduces the predictive controller's tracking accuracy; and stray inductances and resistances in PCB traces, connectors, and cabling introduce unmodeled dynamics that compromise the accuracy of the discrete-time plant model used in the FCS-MPC algorithm. These factors collectively account for the 25% discrepancy between simulation and experiment, underscoring the need for implementation-oriented margins—such as active dead-time compensation—when pursuing IEEE Std. 519-2022 compliance in practical systems.

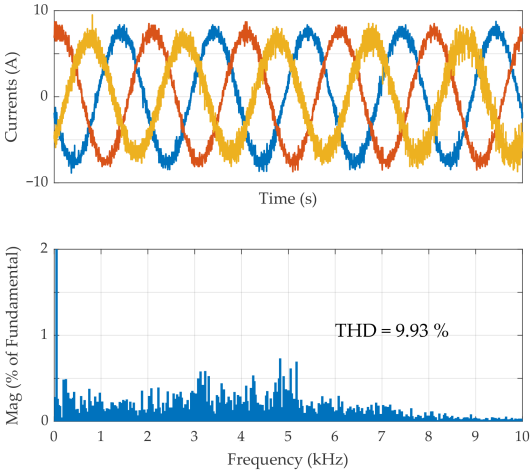


Figure 9. Post-processed load currents and harmonic analysis for the 3L-NPC converter. Top: reconstructed three-phase currents. Bottom: frequency spectrum and THD.

These factors collectively account for the 25% discrepancy between simulation and experiment, underscoring the need for implementation-oriented margins—such as active dead-time compensation—when pursuing IEEE Std. 519-2022 compliance in practical systems. Concerning DC-link capacitor voltage balance, Figure 10 shows the simulated evolution of the two DC-link capacitor voltages V_{dc1} and V_{dc2} obtained under the experimental operating conditions ($V_{dc} = 30$ V, $\lambda = 0.05$). Each capacitor has a nominal reference voltage of $V_{dc}/2 = 15$ V. Under steady-state operation, V_{dc1} stabilizes at approximately 16–17 V while V_{dc2} converges to approximately 14–15 V, yielding a steady-state peak imbalance of $\Delta V_c \approx 3$ V, corresponding to approximately 10% of the total DC-link voltage ($V_{dc} = 30$ V). This higher imbalance relative to the simulated value of 1.92 V (0.48% of $V_{dc} = 400$ V, Table 1) is primarily attributed to practical non-idealities not captured in the ideal simulation model, including IGBT dead-time effects, gate driver propagation delays, and asymmetric switching behavior between the upper and lower converter legs. These results highlight the importance of incorporating active dead-time compensation strategies in future implementations to reduce the simulation-to-experiment discrepancy in DC-link voltage balance performance.

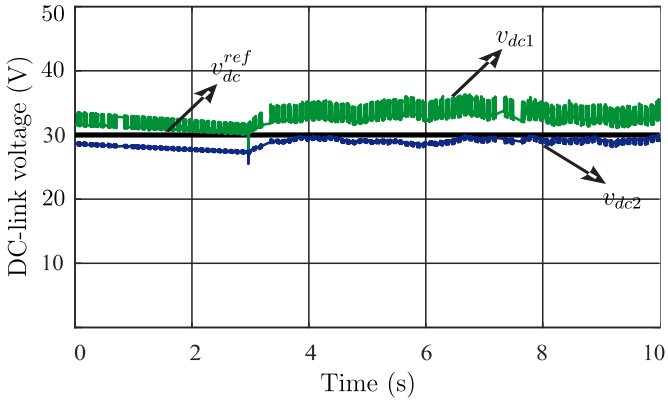


Figure 10. DC-Link capacitor voltage balancing performance obtained from simulation under experimental operating conditions ($V_{dc} = 30$ V, $V_{dc}/2 = 15$ V per capacitor, $\lambda = 0.05$).

3.6. Thermal and Efficiency Considerations

To address the practical operation of the 3L-NPC prototype, a thermal analysis of the switching devices was conducted. The efficiency of the converter is inherently linked to the junction temperature (T_j) of the IGBTs. As T_j increases, the collector–emitter satura-

tion voltage $V_{CE(sat)}$ and switching energy losses (E_{on}, E_{off}) also rise, leading to a slight reduction in overall efficiency. Based on the semiconductor characteristics (SKM50GB12T4), the estimated efficiency at nominal load was 96.4% at an ambient temperature of 25 °C. Under continuous operation where the heatsink temperature reached a steady state of 55 °C, the efficiency slightly adjusted to 95.8%. This variation is mainly attributed to the temperature-dependent conduction losses. Despite these thermal effects, the FCS-MPC algorithm maintained a stable current tracking, and the total harmonic distortion THD remained within the experimental margins reported in Table 5, proving the robustness of the implementation under different thermal conditions.

Table 5. Quantitative comparison between simulation and experimental results.

Parameter	Simulation	Experimental	Error (%)
THD (%)	7.84	9.9	+26.3
ΔV_c (V)	1.92	3.0	+56.2
Settling time (ms)	8	10	+25.0

3.7. Comparison with Simulation

Table 5 presents a quantitative comparison between simulation and experimental results, including the relative error observed in key performance indicators.

It is important to note that the performance of the 5L-NPC converter is assessed exclusively through simulation. However, since both topologies are evaluated using the same predictive control algorithm, identical filter parameters, and equivalent operating conditions, the comparative conclusions regarding harmonic performance and dynamic behavior remain valid. The simulation results, therefore, provide reliable estimates of the expected performance improvement achievable with higher-level topologies. The quantitative comparison presented in Table 6 confirms that while the simulation provides an optimistic lower bound on THD, the experimental result demonstrates the real impact of hardware non-idealities. This gap underscores the need for post-simulation design adjustments—particularly dead-time compensation and improved filtering—when targeting standards compliance in deployed systems [37].

Table 6. Performance Comparison—Simulation vs. Experimental.

Parameter	3L-NPC (Simulation)	3L-NPC (Experimental)	5L-NPC (Simulation)
Grid current THD (%)	7.84	≈9.9	3.36
IEEE 519-2022 Compliance	Marginal	Non-compliant	Satisfied
Power Factor	≈1.0	≈1.0	≈1.0
Dynamic Response	Fast	Fast	Fast
Reactive Power Compensation	Effective	Effective	Effective
Peak ΔV_c	1.92 V (0.48%)	≈3 V (10%) [1]	N/A [2]

[1] Obtained from simulation under experimental operating conditions ($V_{dc} = 30$ V, $V_{dc}/2 = 15$ V per capacitor); see Figure 10. [2] DC-link balance for 5L-NPC assessed qualitatively via simulation; experimental validation is identified as future work.

4. Discussion

4.1. Comparison with Alternative Control Strategies

Table 7 compares FCS-MPC against the main control strategies reported in the literature for grid-connected NPC converters. PI and PR controllers require a dedicated modulation stage and exhibit limited performance under non-linear loads [13,14]. Hysteresis control offers fast response but produces variable switching frequency and poor

THD [16]. SMC provides robustness but is prone to chattering [17]. AI-based approaches achieve competitive THD at the cost of offline training and high implementation complexity [17,38]. CS-MPC requires an additional modulation stage [18]. FCS-MPC uniquely combines fast dynamic response, elimination of the modulation stage, and native multi-objective optimization within a single cost function [16,17,20], making it the most suitable strategy for the NPC-based reactive power compensation evaluated in this work.

Table 7. Comparative overview of control strategies for grid-connected NPC converters. PI: Proportional-Integral; PR: Proportional-Resonant; SMC: Sliding Mode Control; ANN: Artificial Neural Network; CS-MPC: Continuous-Set MPC; FCS-MPC: Finite Control Set MPC.

Strategy	Dynamic Response	THD Performance	Fixed Sw. Freq.	Modulation Stage	Multi-Obj. Opt.	Implementation Complexity
PI/PR [12–14]	Moderate	Moderate	Yes	Yes	No	Low
Hysteresis [16]	Fast	Poor	No	No	No	Low
SMC [17]	Fast	Moderate	No	Yes	Limited	High
AI-based (ANN/Fuzzy) [17,38]	Fast	Good	Variable	Optional	Yes	Very High
CS-MPC [18]	Fast	Good	Yes	Yes	Yes	Moderate
FCS-MPC (This work) [16,17,20]	Fast	Good–Excellent	No	No	Yes	Moderate

4.2. Harmonic Performance

Both topologies demonstrated effective reactive power compensation, reducing the reactive component at the PCC to near-zero in the steady state. However, a significant difference in current waveform quality was observed. The 3L-NPC converter produced a simulated grid current THD of 7.84%, which already exceeds the 5% limit established by IEEE Std. 519-2022 for low-voltage systems, indicating non-compliance even under ideal simulation conditions. The experimental measurement yielded a THD of approximately 9.9%, exceeding this threshold due to practical non-idealities inherent to physical implementations, including IGBT dead-time effects, gate driver propagation delays, and sensor measurement noise. It is worth noting that THD levels above 5% for 3L-NPC converters under FCS-MPC control have also been reported in the literature, particularly when non-ideal implementation effects are taken into account. This behavior is mainly attributed to the finite sampling frequency, the discrete switching nature of FCS-MPC, and the absence of modulation stages, which inherently limit harmonic performance compared to modulation-based strategies. This simulation-to-experiment discrepancy of approximately 25% underscores the importance of incorporating hardware margins when using simulation results as the basis for compliance assessment.

In contrast, the 5L-NPC converter achieved a simulated THD of 3.36%, representing a 57.1% reduction compared to the three-level topology. This improvement is a direct consequence of the finer voltage quantization afforded by five output levels: each switching transition produces a voltage step of $V_{dc}/4$ rather than $V_{dc}/2$, thereby reducing the current ripple amplitude and distributing harmonic energy across a wider frequency range. The resulting waveform more closely approximates the sinusoidal reference, as confirmed by the smoother current profile observed in the simulation results.

It is acknowledged that the simulated THD of the 3L-NPC converter (7.84%) already exceeds the 5% limit established by IEEE Std. 519-2022, even under ideal simulation conditions. This result should be interpreted in the context of the comparative objective of this study: the primary goal is to quantify the relative harmonic improvement achieved by increasing the number of voltage levels, rather than to demonstrate absolute standard compliance for the three-level topology. Nevertheless, compliance with IEEE Std. 519-2022

for the 3L-NPC converter can be achieved through targeted design adjustments. Specifically, increasing the filter inductance Lc beyond the 10 mH value used in this study would reduce the current ripple amplitude and lower THD, but at the cost of a slower dynamic response. Alternatively, reducing the sampling period Ts below 10 µs would increase the effective switching frequency and improve current-tracking accuracy, though this would impose higher computational demands on the real-time control platform. Active dead-time compensation, implemented in software within the FCS-MPC algorithm, constitutes a third viable strategy to mitigate the voltage distortion introduced by IGBT blanking intervals, which was identified as a primary contributor to the simulation-to-experiment discrepancy of approximately 25%. These corrective measures are recommended for future implementations targeting full IEEE Std. 519-2022 compliance under practical operating conditions, and their implications from the perspectives of computational complexity and hardware implementation are analyzed in the following sections.

4.3. Dynamic Response

Beyond harmonic performance, the dynamic response of the FCS-MPC controller was evaluated by analyzing the transient behavior of the compensating current upon activation of the compensator. In the 3L-NPC simulation, the grid current reached steady-state compensation within approximately $t_{ss} \approx 8$ ms after the compensator was enabled, with no observable overshoot in the reactive current trajectory. The experimental prototype exhibited a comparable settling time of $t_{ss} \approx 10$ ms, with the slight increase attributable to gate driver propagation delays and the finite rise time of the IGBT switches. These results confirm the fast-transient capability of the FCS-MPC strategy, which is inherent to its single-step prediction horizon and to the direct selection of the optimal switching state at each sampling instant [17].

4.4. Computational Complexity

The FCS-MPC algorithm selects the optimal switching state by exhaustively evaluating all admissible converter states at each sampling instant. The number of states to be evaluated is determined by the number of output voltage levels and the number of phases, according to $N = L^3$, where L is the number of levels.

As shown in Table 8, the transition from the three-level to the five-level topology increases the number of switching states evaluated per sampling period from 27 to 125, representing a 4.6× increase in the computational burden of the FCS-MPC algorithm. This imposes substantially higher demands on the digital control platform, requiring either a higher-performance processor or reduced-search strategies to maintain real-time execution within the sampling period [39].

Table 8. Comparative summary of 3L-NPC and 5L-NPC converter topologies under FCS-MPC.

Parameter	3L-NPC	5L-NPC
Output voltage levels	3	5
Switching states (N)	27	125
Relative computational load	1×	4.6×
IGBTs per phase leg	4	8
Clamping diodes per phase	2	6
DC-link capacitors	2	4

4.5. Hardware Implementation Cost

Beyond computational demands, the 5L-NPC topology entails a significant increase in hardware complexity. Each phase leg requires twice the number of active switches (8 vs. 4 IGBTs) and three times the number of clamping diodes (6 vs. 2), while the DC-link

bus requires four series capacitors instead of two [40]. This increase in component count raises material cost, board area, thermal management requirements, and the probability of component failure. Furthermore, maintaining balanced voltages across four DC-link capacitors is considerably more challenging than in the three-level case, increasing the relative importance of the voltage balance term $\lambda \Delta V_c$ in the cost function.

Consequently, the selection of an appropriate topology depends on the trade-off between power quality requirements and implementation constraints. The 3L-NPC converter is well suited for applications with moderate harmonic requirements and cost or complexity constraints, provided that active dead-time compensation is applied to bring experimental THD within IEEE Std. 519-2022 limits. The 5L-NPC converter is preferable in systems where strict harmonic compliance, high waveform quality, and energy efficiency are priorities, and where a more capable digital control platform is available [22,38,41–43].

4.6. DC-Link Capacitor Voltage Balance

The DC-link capacitor voltage balance constitutes a critical operational constraint in NPC converters, directly affecting output waveform quality, semiconductor voltage stress, and overall system reliability. In this study, the $\lambda \Delta V_c$ penalty term in the cost function provided active regulation of the neutral-point voltage in both evaluated topologies.

For the 3L-NPC converter in simulation, the balance metric is defined as $\Delta V_c = |V_{dc1} - V_{dc2}|$, where each capacitor must be maintained at $V_{dc}/2 = 200$ V. With $\lambda = 0.05$, the steady-state peak imbalance reached $\Delta V_c = 1.92$ V (0.48% of $V_{dc} = 400$ V), as reported in Table 1, confirming that the selected weighting factor achieves adequate capacitor voltage regulation while preserving current tracking quality, as evidenced by the THD results reported in Section 3.

Under the experimental operating conditions, Figure 10 shows the simulation results for V_{dc1} and V_{dc2} obtained with $V_{dc} = 30$ V and $\lambda = 0.05$, where each capacitor has a nominal reference of $V_{dc}/2 = 15$ V. V_{dc1} stabilizes at approximately 16–17 V while V_{dc2} converges to 14–15 V, yielding a steady-state imbalance of $\Delta V_c \approx 3$ V (10% of $V_{dc} = 30$ V), as summarized in Table 6. This represents a simulation-to-experiment discrepancy in balance performance analogous to the THD discrepancy reported in Section 3.5, and is similarly attributable to hardware non-idealities including IGBT dead-time effects and asymmetric gate driver delays between the upper and lower converter legs, which introduce systematic voltage offsets not represented in the ideal discrete-time plant model used by the FCS-MPC algorithm.

For the 5L-NPC topology, the balancing problem is inherently more demanding, as four series capacitors must be regulated at $V_{dc}/4 = 100$ V each. The balance error is defined over two capacitor pairs as $\Delta V_c = (V_{C1} + V_{C2}) - (V_{C3} + V_{C4})$, as implemented in the predictive model. The cost function penalty term remains effective for this topology under simulation conditions; however, the increased number of capacitors raises the sensitivity of the balance term to switching state selection. Topology-specific tuning of λ or adaptive weighting strategies may therefore be beneficial in future implementations targeting stricter voltage balance tolerances, and constitute an identified direction for future work alongside the experimental validation of the 5L-NPC prototype.

4.7. Comparison with Related Works

Table 9 summarizes selected recent works on NPC converter topologies operating under model predictive control strategies, providing context for the contributions of the present study.

Table 9. Comparison with Related Works on NPC Converters under Predictive Control.

Reference	Topology	Control	Application	THD (%)	Experimental
[20]	3L-NPC	FCS-MPC	Current control	–	Yes
[21]	3L-NPC	FCS-MPC	Power quality	–	No
[44]	3L-NPC	FCS-MPC	Fixed switching freq	<5	Yes
[19]	3L-NPC	FCS-MPC	Reduced states	–	Yes
[7]	3L-NPC	MPC	Reactive compensation	–	Yes
This work	3L/5L-NPC	FCS-MPC	Reactive compensation	3.36/7.84	Yes (3L)

As shown in Table 9, most related work focuses on the 3L-NPC topology, with experimental validation reported in several cases [7,19–21,44]. The present work extends this body of knowledge by providing a direct simulation-based comparison between the 3L-NPC and 5L-NPC topologies under identical FCS-MPC conditions, combined with experimental validation of the three-level prototype. The 5L-NPC topology achieves a simulated THD of 3.36%, the lowest reported value among the works listed, while the experimental 3L-NPC result of 9.8% quantifies the implementation gap introduced by hardware non-idealities that are not captured in simulation-only studies.

These results highlight that, beyond numerical performance differences, the choice of converter topology directly impacts implementation feasibility and control robustness. In practical applications, the increased harmonic performance of the 5L-NPC must be weighed against its higher computational burden and hardware complexity. Moreover, the observed discrepancies between simulation and experimental results emphasize the importance of considering non-ideal effects during the design stage, as these factors can significantly affect compliance with power quality standards in real-world deployments. From a system-level perspective, these findings confirm that increasing the number of voltage levels constitutes an effective strategy to enhance power quality, although at the expense of increased control and implementation complexity.

5. Conclusions

This study presents a comparative evaluation of three-level and five-level Neutral-Point-Clamped (NPC) converters under Finite Control Set Model Predictive Control (FCS-MPC) for reactive power compensation in a three-phase inductive load system. Both topologies achieved effective reactive power compensation and near-unity power factor at the PCC. However, harmonic performance differed significantly: the 3L-NPC converter yielded a simulated grid current THD of 7.84% and an experimental THD of approximately 9.9%, exceeding the 5% limit established by IEEE Std. 519-2022, while the 5L-NPC topology achieved 3.36% in simulation, fully satisfying the standard and confirming the harmonic advantages of higher-resolution multilevel topologies.

The experimental validation of the 3L-NPC prototype, conducted on a dSPACE MicroLabBox real-time platform, revealed a simulation-to-experiment discrepancy of approximately 25%, attributable to hardware non-idealities, including IGBT dead time, gate driver propagation delays, and measurement noise introduced by the signal acquisition chain. To address the latter, custom-designed sensor boards were developed and validated, incorporating the CS60-100L current transformer and the AMC1350 galvanically isolated instrumentation amplifier for current measurement, and a resistive divider-based circuit with AMC1350 isolation for voltage acquisition. Both boards feature anti-aliasing filtering at 48.2 kHz and isolated DC-DC power supplies, ensuring high signal integrity and electromagnetic compatibility in the switching environment of the converter. These hardware

contributions constitute a practical instrumentation framework that is replicable on similar power electronics experimental platforms.

The results demonstrate a clear performance–complexity trade-off between the evaluated topologies. The 3L-NPC converter offers a simpler structure and lower hardware cost, but requires active dead-time compensation and improved filtering to achieve IEEE Std. 519-2022 compliance under real operating conditions. Conversely, the 5L-NPC converter delivers superior waveform quality and harmonic compliance at the expense of a 4.6× increase in FCS-MPC computational burden and significantly higher component count, including twice the number of active switches and four DC-link capacitors per phase leg. The main limitation of this work is the absence of experimental validation for the 5L-NPC topology. Nevertheless, this does not compromise the validity of the comparative analysis, as both converter topologies are evaluated under identical control strategies, system parameters, and operating conditions. The experimentally validated 3L-NPC prototype provides a reliable reference framework, while the 5L-NPC simulation results offer a consistent, theoretically grounded estimate of the performance improvements achievable with higher voltage levels. Future research will address this gap by implementing and validating the five-level prototype under the same instrumentation framework, extending the comparative analysis to alternative architectures such as Active Neutral-Point-Clamped (ANPC) converters, and exploring reduced-search FCS-MPC strategies to alleviate computational demands while preserving harmonic performance.

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Abbreviations

The following abbreviations are used in this manuscript:

NPC	Neutral Point Clamped
3L-NPC	Three-Level Neutral-Point-Clamped Converter
5L-NPC	Five-Level Neutral-Point-Clamped Converter
FCS-MPC	Finite Control Set Model Predictive Control
THD	Total Harmonic Distortion
PCC	Point of Common Coupling
STATCOM	Static Synchronous Compensator
FACTS	Flexible AC Transmission Systems
IGBT	Insulated Gate Bipolar Transistor
RL	Resistor–Inductor (load or filter)
FFT	Fast Fourier Transform

Appendix A. Extended Experimental and Simulation Parameters

This appendix provides additional details of the experimental setup and simulation parameters used in the study. Figures 4 and 9 show the complete schematic of the laboratory prototype and the extended FFT analysis of the measured grid current.

Table A1. Extended Simulation Parameters.

Parameter	Value	Notes
Switching frequency	10 kHz	Applied in both 3L-NPC and 5L-NPC
Dead-time	2 µs	Introduced in experimental prototype
Sensor resolution	12 bits	Current and voltage acquisition

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